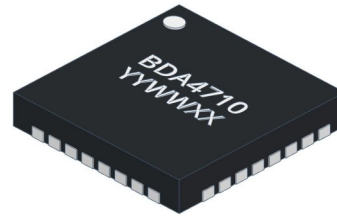


Device Features

- 7-bit Serial & Parallel Interface
- 31.75 dB Control Range 0.25 dB step
- Support addressable Function (Addr0-Addr7)
- Glitch-safe attenuation state transitions
- 2.7 V to 5.5 V supply
- 1.8 V or 3.3 V control logic
- Excellent Attenuation Accuracy
Any bit Attenuation Error < ± 0.5 dB up to 6GHz
- Low Insertion Loss
 - 0.6 dB @ 1GHz
 - 0.8 dB @ 2GHz
 - 1.1 dB @ 3GHz
 - 1.4 dB @ 4GHz
 - 2.0 dB @ 5GHz
 - 2.6 dB @ 6GHz
 - 2.7 dB @ 7GHz
- Ultra linearity IIP3 > +68 dBm @ 3.5GHz, ATT=0dB
- Input 0.1dB Compression (P0.1dB) 30dBm @ 3.5GHz, ATT=0dB
- Programming modes
 - Direct parallel
 - Latched parallel
 - Serial Addressable
- Stable Integral Non-Linearity over temperature
- Low Current Consumption 200 μ A typical
- -40 °C to +105 °C operating temperature
- ESD rating : Class1C (1KV HBM)
- Lead-free/RoHS2-compliant 32-lead 5mm x 5mm x 0.9mm QFN SMT package



32-lead 5mm x 5 mm x 0.9mm QFN

Figure 1. Package Type

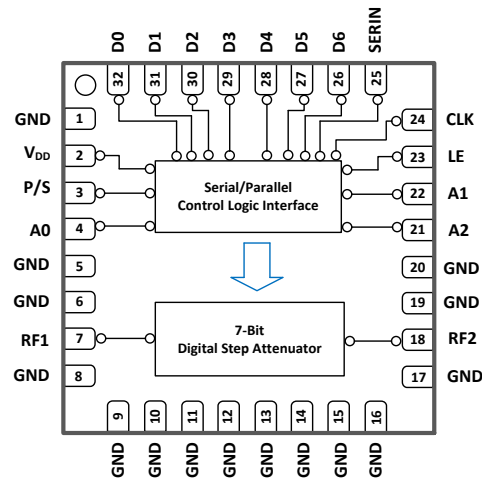


Figure 2. Functional Block Diagram

Product Description

The BDA4710 is a broadband, Highly accurate 50 Ω digital step attenuator model which provides adjustable attenuation from 0 to 31.75 dB in 0.25 dB steps. The control interface supports a 7-bit serial interface with 3-bit addressable function and latched parallel interface.

BDA4710 supports a broad operating frequency range from 1MHz to 8.0 GHz. BDA4710 is offering the High linearity, low power consumption, low insertion loss, high attenuation accuracy and low insertion loss less than 2.8dB typical at all frequency band.

The device features a safe state transitions with no negative/positive Glitch technology optimized for excellent step accuracy.

The RF input and output are internally matched to 50 Ω and do not require any external matching components. The design is bi-directional; Therefore, the RF input and output are interchangeable.

The BDA4710 does not require blocking capacitors. If DC is presented at the RF port, add a blocking capacitor. This is packaged in a RoHS2-compliant with QFN surface mount package.

Application

- 5G/4G+/4G/3G Cellular Base station/Repeater Infrastructure
- Digital Pre-Distortion
- Distributed Antenna Systems, DAS
- Remote Radio Heads
- NFC Infrastructure
- Test Equipment and sensors
- Military Wireless system
- Cable Infrastructure
- General purpose Wireless

7-bit Digital Step Attenuator with Addressable Function
1MHz – 8GHz
Table 1. Electrical Specifications¹

| Parameter | Condition | Frequency | Min | Typ | Max | Unit | |
|-----------------------------|--------------------------------------|-------------------------------|---------------|-----------|------|-------------------------------------|----|
| Operational Frequency Range | | | 1 | | 8000 | MHz | |
| Attenuation range | 0.25dB step | | | 0 - 31.75 | | dB | |
| Insertion Loss ² | ATT = 0dB | 1MHz - 1GHz | | 0.6 | 0.7 | dB | |
| | | > 1 - 2.2GHz | | 0.7 | 0.8 | dB | |
| | | > 2.2 - 4GHz | | 1.1 | 1.4 | dB | |
| | | > 4 - 6GHz | | 2.0 | 2.7 | dB | |
| | | > 6 - 8GHz | | 2.8 | 2.8 | dB | |
| Attenuation Error | 0.25dB Step | 0-31.75dB | 1MHz - 2.2GHz | | | ±(0.15 + 1.5% of attenuation state) | dB |
| | | | > 2.2 - 3GHz | | | ±(0.15 + 2.5% of attenuation state) | |
| | | | > 3 - 5GHz | | | ±(0.25 + 3.5% of attenuation state) | |
| | | | > 5 - 6GHz | | | ±(0.25 + 5.0% of attenuation state) | |
| | | | | | | | |
| | 1dB Step | 0-31.0dB | 1MHz - 2.2GHz | | | ±(0.15 + 1.5% of attenuation state) | dB |
| | | | > 2.2 - 3GHz | | | ±(0.15 + 2.5% of attenuation state) | |
| | | | > 3 - 5GHz | | | ±(0.25 + 3.5% of attenuation state) | |
| | | | > 5 - 6GHz | | | ±(0.25 + 5.0% of attenuation state) | |
| | | | > 6 - 8GHz | | | ±(0.25 + 7.0% of attenuation state) | |
| Input Return Loss | ATT = 0dB | 1 - 4GHz | | 20 | | dB | |
| | | > 4 - 8GHz | | 9 | | | |
| Output Return Loss | ATT = 0dB | 1 - 4GHz | | 21 | | dB | |
| | | > 4 - 8GHz | | 9 | | | |
| Relative Phase Error | All States | 1GHz | | 7 | | degree | |
| | | 2GHz | | 14 | | | |
| | | 3GHz | | 22 | | | |
| | | 4GHz | | 31 | | | |
| | | 5GHz | | 39 | | | |
| | | 6GHz | | 47 | | | |
| Input Linearity | Input 0.1dB Compression point | ATT = 0dB | 3.5GHz | 30 | | dBm | |
| | | Pin = +18dBm/tone, Δf = 20MHz | 2.5GHz | 63 | | | |
| | ATT = 0.0dB RF Input = RF1 Port | 3.5GHz | 68 | | | | |
| | | 4.5GHz | 59 | | | | |
| | | 7.25GHz | 52 | | | | |
| | | Pin = +18dBm/tone, Δf = 20MHz | 2.5GHz | 59 | | | |
| | ATT = 31.75dB RF Input = RF1 Port | 3.5GHz | 58 | | | | |
| | | 4.5GHz | 54 | | | | |
| | | 7.25GHz | 51 | | | | |
| | | Pin = +18dBm/tone, Δf = 20MHz | 2.5GHz | 64 | | | |
| | ATT = 0.0dB RF Input = RF2 Port | 3.5GHz | 60 | | | | |
| | | 4.5GHz | 58 | | | | |
| | | 7.25GHz | 49 | | | | |
| | | Pin = +18dBm/tone, Δf = 20MHz | 2.5GHz | 58 | | | |
| | ATT = 31.75dB RF Input = RF2 Port | 3.5GHz | 57 | | | | |
| | | 4.5GHz | 56 | | | | |
| 7.25GHz | | 42 | | | | | |

Preliminary Datasheet

Table 1. Electrical Specifications¹(Cont.)

| Parameter | Condition | Frequency | Min | Typ | Max | Unit |
|---|--|-----------|-----|--------|-----|------|
| RF Rising / Falling Time | 10%/90% RF | 2GHz | | 121 | | ns |
| Switching time | 50% CTRL to 90% or 10% RF | 2GHz | | 224 | | ns |
| Settling time | 50% CTRL to Max or Min Attenuation to settle within 0.05 dB of final value | 2GHz | | 500 | | ns |
| Attenuation Transient (envelope) ³ | Positive glitch, Any ATT step | 3.5GHz | | 0.3 | | dB |
| Maximum Spurious level ⁴ | Measured at RF ports | < 7MHz | | < -145 | | dBm |

1. Device performance is measured on a BeRex Evaluation board Kit at 25°C, 50 Ω system, VDD=+3.3V

2. The Evaluation board Kit insertion loss (PCB & RF Connector) is de-embedded.

3. Attenuation Transient is glitch level due to attenuation transitions

4. The unwanted spurious due to built-in negative voltage generator. Typical generated fundamental frequency is 6.8MHz.

Table 2. Recommended operating Condition

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|-----------------------------|--------------------|-------------------|-----------------------------|------|-----|------|
| Supply Voltages | V _{DD} | | 2.7 | | 5.5 | V |
| Supply Current | I _{DD} | | | 200 | 300 | μA |
| Digital Control Input | High | V _{CTLH} | V _{DD} =3.3V or 5V | 1.17 | 3.6 | V |
| | Low | V _{CTLL} | V _{DD} =3.3V or 5V | -0.3 | 0.6 | V |
| Operating Temperature Range | T _{Case} | Exposed Paddle | -40 | | 105 | °C |
| RF Max Input Power | P _{IN_CW} | RF1 or RF2, CW | | | 23 | dBm |
| Impedance | Z _{Load} | Single ended | | 50 | | Ω |

Specifications are not guaranteed over all recommended operating conditions.

Table 3. Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Unit |
|-----------------------|-----------------------|--------------------|-----|--------------------|------|
| Supply Voltage | V _{DD} | -0.3 | | 5.5 | V |
| Digital input voltage | V _{CTL} | -0.3 | | 3.6 | V |
| Maximum input power | P _{IN_CWMAX} | | | 34 | dBm |
| Temperature | Storage | T _{ST} | -65 | 150 | °C |
| | Reflow | T _R | | 260 | °C |
| ESD Sensitivity | HBM ¹ | ESD _{HBM} | | 1000 (Class 1C) | V |
| | CDM ² | ESD _{CDM} | | 1000 (Class C4) | V |

Operation of this device above any of these parameters may result in permanent damage.

1. HBM : Human Body Model (JEDEC Standard JS-001-2017)

2. CDM : Charged Device Model (JEDEC Standard J-STD-020)

Figure 3. Pin Configuration (Top View)

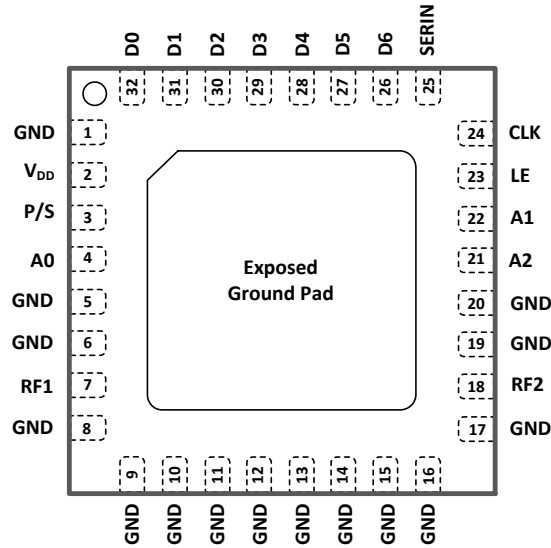


Table 4. Pin Description

| Pin | Pin name | Description |
|----------------------|------------------|---|
| 1, 5, 6, 8-17, 19,20 | GND | Ground, These pins must be connected to ground |
| 2 | VDD | Power Supply (nominal 3.3V) |
| 3 | P/S | Parallel/Serial Mode Select. For parallel mode operation, set this pin to LOW. For serial mode operation, set this pin to HIGH. |
| 4 | A0 | Address bit A0 connection. |
| 5 | RF1 ¹ | RF1 port (Attenuator RF Input) This pin can also be used as an output because the design is bidirectional. RF1 is dc-coupled and matched to 50 Ω |
| 18 | RF2 ¹ | RF2 port (Attenuator RF Output.) This pin can also be used as an input because the design is bidirectional. RF2 is dc-coupled and matched to 50 Ω. |
| 21 | A2 | Address bit A2 connection. |
| 22 | A1 | Address bit A1 connection. |
| 23 | LE | Latch Enable input |
| 24 | CLK | Serial interface clock input |
| 25 | SERIN | Serial interface data input |
| 26 | D6 ² | Parallel Control Voltage Inputs, Attenuation control bit 16dB |
| 27 | D5 ² | Parallel Control Voltage Inputs, Attenuation control bit 8dB |
| 28 | D4 ² | Parallel Control Voltage Inputs, Attenuation control bit 4dB |
| 29 | D3 ² | Parallel Control Voltage Inputs, Attenuation control bit 2dB |
| 30 | D2 ² | Parallel Control Voltage Inputs, Attenuation control bit 1dB |
| 31 | D1 ² | Parallel Control Voltage Inputs, Attenuation control bit 0.5dB |
| 32 | D0 ² | Parallel Control Voltage Inputs, Attenuation control bit 0.25dB |
| Pad | GND | Exposed pad: The exposed pad must be connected to ground for proper operation |

1. RF pins 5 and 18 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper Operation if the 0V DC requirement is met
 2. Ground D0 - D6 if not used or serial mode.

Programming Options

BDA4710 can be programmed using either the parallel or serial interface, which is selectable via P/S pin(Pin3).

Serial mode is selected by pulling it to a voltage logic HIGH and parallel mode is selected by setting P/S to logic LOW

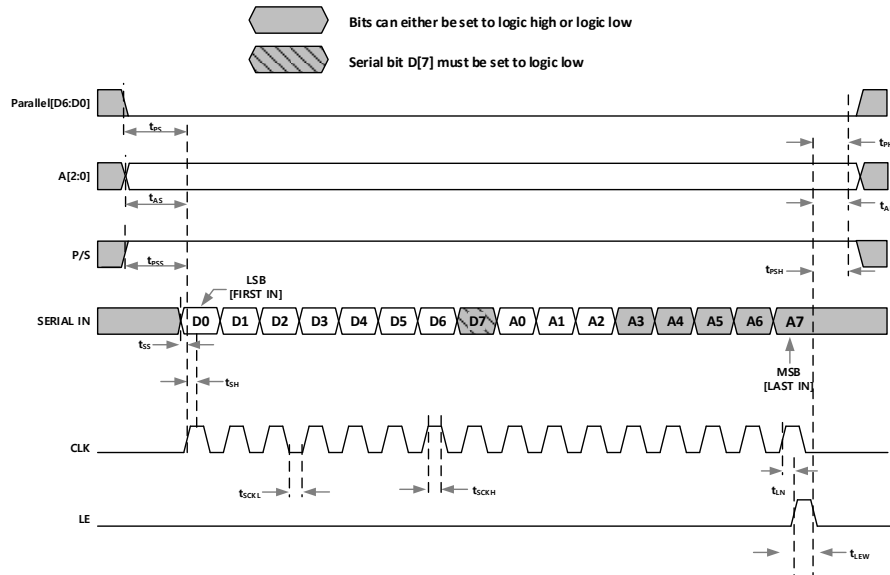
Serial Control Mode

The serial interface is a 7-bit shift register to shift in the data LSB (D0) first. When serial programming is used, It is recommended all the parallel control input pins (26, 27, 28, 29, 30, 31, 32) are grounded. It is controlled by three CMOS-compatible signals: SERIN, Clock, and Latch Enable (LE).

Table 5. Truth Table for Serial Control Word

| Digital Control Input | | | | | | | | Attenuation state (dB) |
|-----------------------|------|------|------|------|------|------|----------|------------------------|
| D7 (MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 (LSB) | |
| LOW | LOW | LOW | LOW | LOW | LOW | LOW | LOW | 0 (RL) |
| LOW | LOW | LOW | LOW | LOW | LOW | LOW | HIGH | 0.25 |
| LOW | LOW | LOW | LOW | LOW | LOW | HIGH | LOW | 0.5 |
| LOW | LOW | LOW | LOW | LOW | HIGH | LOW | LOW | 1.0 |
| LOW | LOW | LOW | LOW | HIGH | LOW | LOW | LOW | 2.0 |
| LOW | LOW | LOW | HIGH | LOW | LOW | LOW | LOW | 4.0 |
| LOW | LOW | HIGH | LOW | LOW | LOW | LOW | LOW | 8.0 |
| LOW | HIGH | LOW | LOW | LOW | LOW | LOW | LOW | 16.0 |
| LOW | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | 31.75 |

Figure 4. Serial Mode Resister Timing Diagram



BDA4710 Serial mode is selected by pulling it to logic HIGH. The serial interface is a 16-bit shift register made up of two words. The first 8-bit word is the Attenuation word, which controls the DSA state. The second word is the address word, which uses only 3 of 8-bits that must match the hard wired A0-A2 programming in order to change the DSA state. If no external connections are made to A0 – A2 then internally they will default to 000 due to internal pull down resistors. If these 3 external preset address bits are not matched with the SPI loaded address bits then the current attenuator state will remain unchanged. This allows up to 8 serial-controlled devices to be used on a single board, which share a common SERIN, CLK and LE.

When serial programming is used, all the parallel control input pins 26 – 32 can be left open or grounded.

Table 6. Serial Interface Timing Specifications

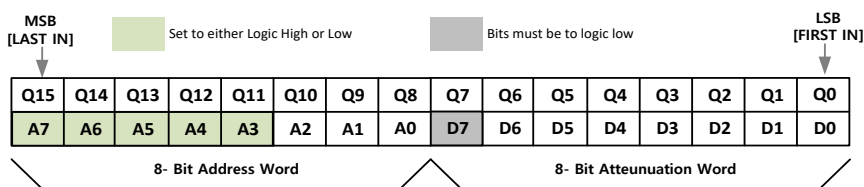
| Symbol | Parameter | Min | Typ | Max | Unit |
|------------|-----------------------------|-----|-----|-----|------|
| f_{CLK} | Serial data clock frequency | | | 10 | MHz |
| t_{PS} | Parallel data setup time | 100 | | | ns |
| t_{PH} | Parallel data hold time | 100 | | | ns |
| t_{AS} | Address setup time | 100 | | | ns |
| t_{AH} | Address hold time | 100 | | | ns |
| t_{PSS} | Parallel/Serial setup time | 100 | | | ns |
| t_{PSH} | Parallel/Serial hold time | 100 | | | ns |
| t_{SS} | Serial Data setup time | 10 | | | ns |
| t_{SH} | Serial Data hold time | 10 | | | ns |
| t_{SCKH} | Serial clock high time | 30 | | | ns |
| t_{SCKL} | Serial clock low time | 30 | | | ns |
| t_{LN} | LE setup time | 10 | | | ns |
| t_{LEW} | Minimum LE pulse width | 30 | | | ns |

Serial Register Map

The BDA4710 can be programmed via the serial control on the rising edge of Latch Enable (LE) which loads the last 8-bits attenuation word and 8-bits address word in the SHIFT Register. Data is clocked in LSB(D0) first.

The shift register must be loaded while LE is kept LOW to prevent changing the attenuation value during data is inputted.

Figure 5. Serial Register Map



The serial register consist of 16 bits as shown in Figure 5. First 8 bits from LSB are Attenuation word, 8 bits after that are Address word. The Attenuation word is DSA attenuation control bit and the Address word is static logical bit determined by A0, A1 and A2 digital inputs. The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four because of 0.25dB step up to 31.75dB (total 127 Attenuation state), then convert to binary.

For example, to program attenuation 15.75dB state of Addr[5] BDA4710 :

| | |
|-------------------|---------------------------------------|
| Attenuation State | Address state |
| 4 x 15.75 = 63 | Digital input of A2, A1, A0 pin = 101 |
| 63 -> 00111111 | A7 - A0 : xxxxx101 |

Serial Input : xxxxx10100111111

| | | | | | | | | | | | | | | | |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| x | x | x | x | x | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Table 7. Truth Table for Address Control Word

| Address Digital Control Input | | | | | | | | Address Setting | Addr No. |
|-------------------------------|----|----|----|----|------|------|----------|-----------------|----------|
| A7 (MSB) | A6 | A5 | A4 | A3 | A2 | A1 | A0 (LSB) | | |
| X | X | X | X | X | LOW | LOW | LOW | 000 | Addr[0] |
| X | X | X | X | X | LOW | LOW | HIGH | 001 | Addr[1] |
| X | X | X | X | X | LOW | HIGH | LOW | 010 | Addr[2] |
| X | X | X | X | X | LOW | HIGH | HIGH | 011 | Addr[3] |
| X | X | X | X | X | HIGH | LOW | LOW | 100 | Addr[4] |
| X | X | X | X | X | HIGH | LOW | HIGH | 101 | Addr[5] |
| X | X | X | X | X | HIGH | HIGH | LOW | 110 | Addr[6] |
| X | X | X | X | X | HIGH | HIGH | HIGH | 111 | Addr[7] |

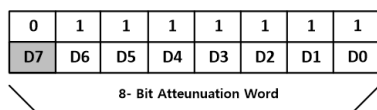
Table 8. Mode Selection

| P/S | Control Mode |
|------|--------------|
| LOW | Parallel |
| HIGH | Serial |

Power-UP states Settings

The BDA4710 will always initialize to the maximum attenuation setting (31.75 dB) on power-up for both the Serial and Latched Parallel modes of operation and will remain in this setting until the user latches in the next programming word. In Direct Parallel mode, the DSA can be preset to any state within the 31.75 dB range by pre-setting the Parallel control pins prior to power-up. In this mode, there is a 400 μs delay between the time the DSA is powered-up to the time the desired state is set.

Figure 6. Default Attenuation Word for Power-up state



Programming Options

Parallel Control Mode

The parallel control interface has seven digital control input lines (D6 to D0) to set the attenuation value. D6 is the most significant bit (MSB) that selects the 16 dB attenuator stage, and D0 is the least significant bit (LSB) that selects the 0.25 dB attenuator stage (see Figure 7).

Direct Parallel Mode

For direct parallel mode, The LE pin must be kept HIGH. The attenuation state is changed by the control voltage inputs (D0 to D6) directly. This mode is ideal for manual control of the attenuator. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 26, 27, 28, 29, 30, 31, 32]. Use direct parallel mode for the fastest settling time. (refer to page 21)

Latched Parallel Mode

The LE pin must be kept LOW when changing the control voltage inputs (D0 to D6) to set the attenuation state. When the desired state is set, LE must be toggled HIGH to transfer the 7-bit data to the bypass switches of the attenuator array, and then toggled LOW to latch the change into the device until the next desired attenuation change (see Figure 7 and Table 8).

- Set P/S is logic LOW.
- Set LE to logic LOW.
- Adjust pins [26, 27, 28, 29, 30, 31, 32] to the desired attenuation setting. (Note the device will not react to these pins while LE is a logic LOW).
- Pull LE to a logic HIGH. The device will then transition to the attenuation settings reflected by pins D6 - D0.
- If LE is pulled to a logic LOW then the attenuator will not change state.

Latched Parallel Mode implies a default state for when the device is first powered up with P/S pin set for logic LOW and LE logic LOW. In this case the default setting is **Maximum attenuation**.

Switching Feature Description

Glitch-Safe Attenuation State Transient

The BDA4710 is the latest product applied *Glitch-Safe* technology with less than 1dB ringing (pos/neg) across the attenuation range when changing attenuation states. This technology protects Amplifiers or ADC during transitions between attenuation states. (see Figure 40,41).

Table 9. Truth Table for the Parallel Control Word

| D6 | D5 | D4 | D3 | D2 | D1 | D0 | P/S | LE | Attenuation State(dB) |
|------|------|------|------|------|------|------|-----|------|-----------------------|
| LOW | LOW | LOW | LOW | LOW | LOW | LOW | LOW | HIGH | 0 (RL) |
| LOW | LOW | LOW | LOW | LOW | LOW | HIGH | LOW | HIGH | 0.25 |
| LOW | LOW | LOW | LOW | LOW | HIGH | LOW | LOW | HIGH | 0.5 |
| LOW | LOW | LOW | LOW | HIGH | LOW | LOW | LOW | HIGH | 1.0 |
| LOW | LOW | LOW | HIGH | LOW | LOW | LOW | LOW | HIGH | 2.0 |
| LOW | LOW | HIGH | LOW | LOW | LOW | LOW | LOW | HIGH | 4.0 |
| LOW | HIGH | LOW | LOW | LOW | LOW | LOW | LOW | HIGH | 8.0 |
| HIGH | LOW | LOW | LOW | LOW | LOW | LOW | LOW | HIGH | 16.0 |
| HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | LOW | HIGH | 31.75 |

Figure 7. Latched Parallel Mode Timing Diagram

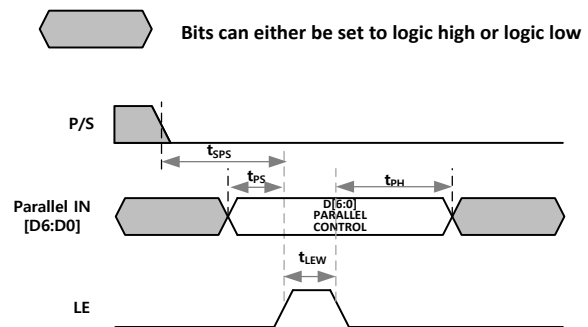


Table 10. Parallel Interface Timing Specifications

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|------------------------------------|-----|-----|-----|------|
| t_{SPS} | Serial to Parallel Mode Setup Time | 100 | | | ns |
| t_{LEW} | Minimum LE pulse width | 10 | | | ns |
| t_{PH} | Data hold time from LE | 10 | | | ns |
| t_{PS} | Data setup time to LE | 10 | | | ns |

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 8. Insertion loss vs Temperature

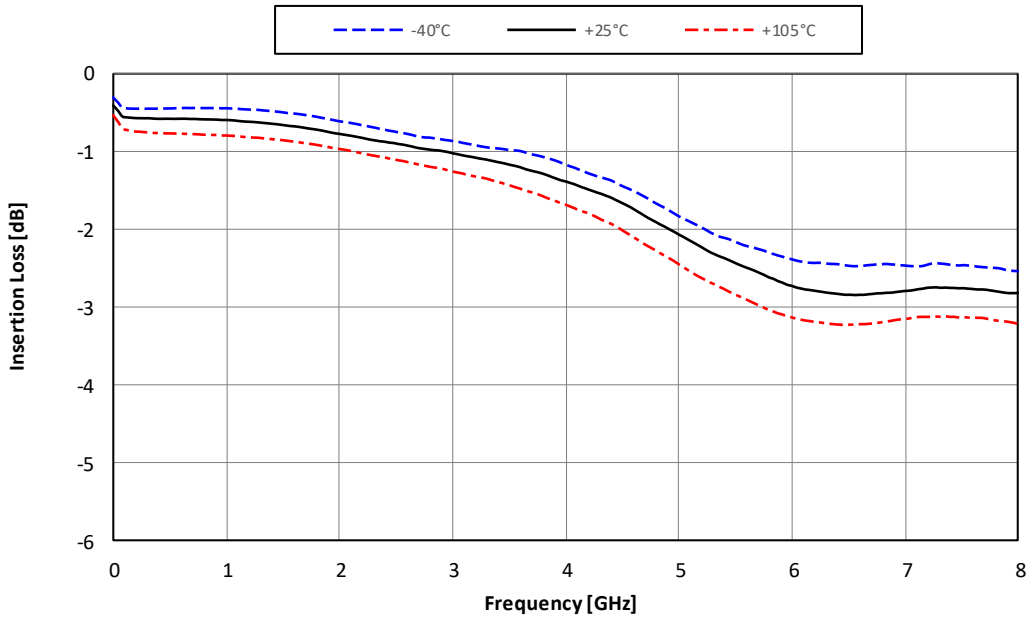
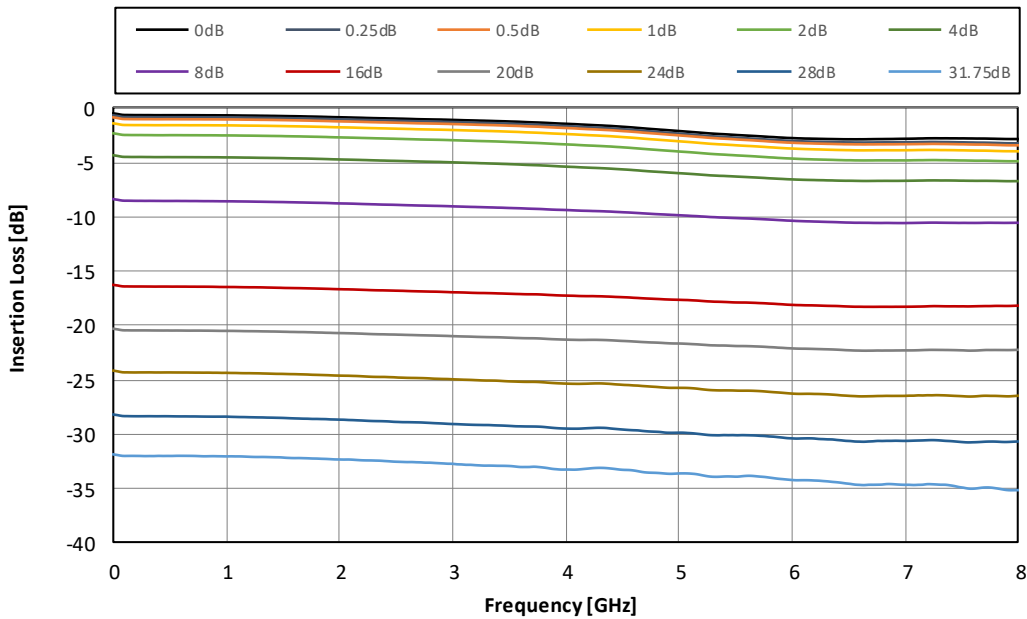


Figure 9. Insertion loss vs Attenuation Setting



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 10. Input Return Loss vs Attenuation Setting

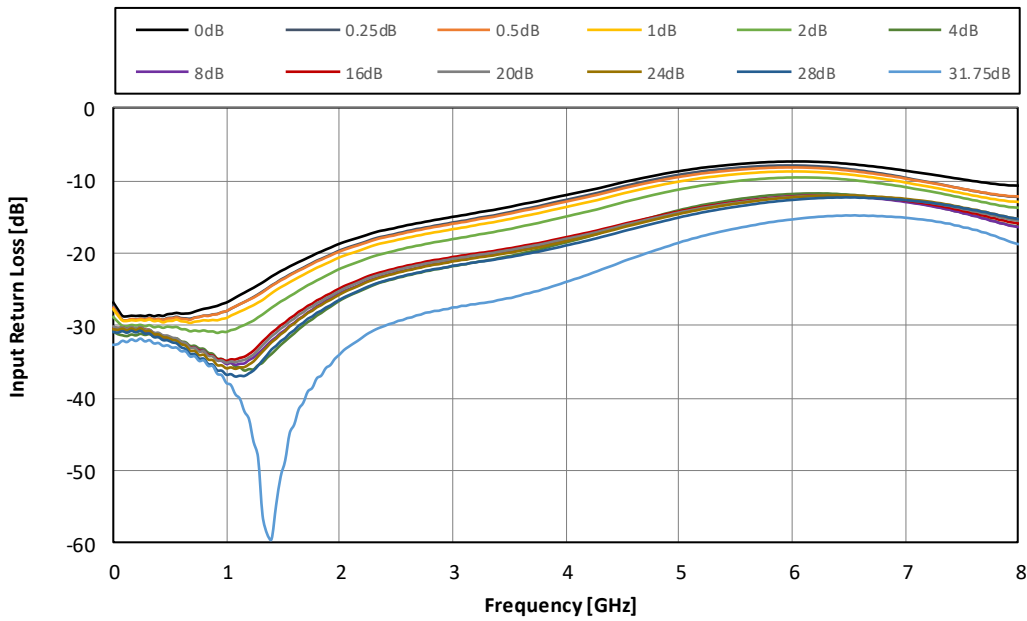
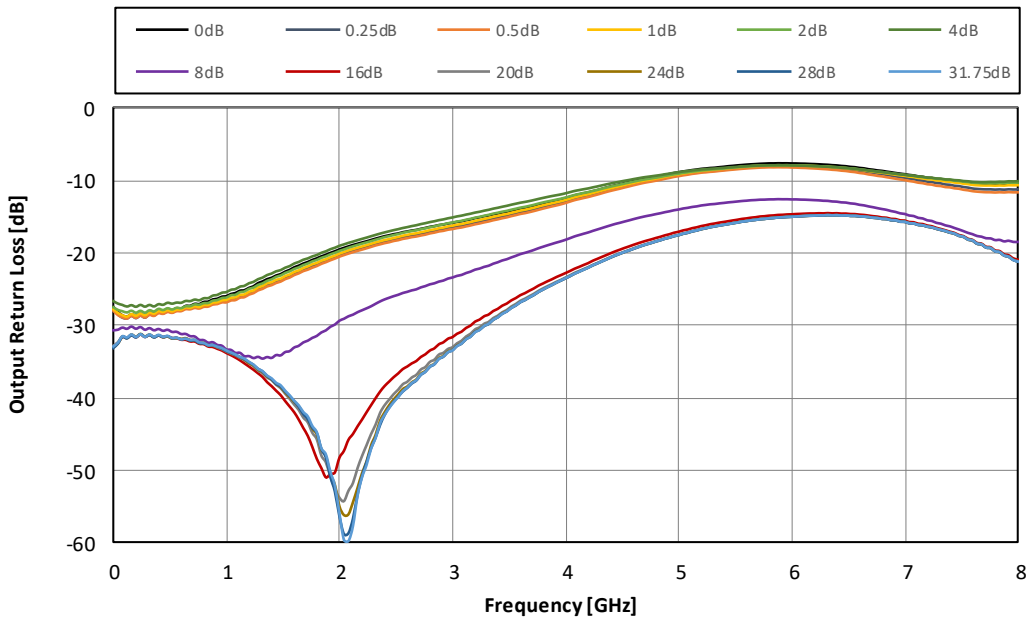


Figure 11. Output Return Loss vs Attenuation Setting



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 12. Input Return Loss for 16dB Attenuation Setting vs Temperature

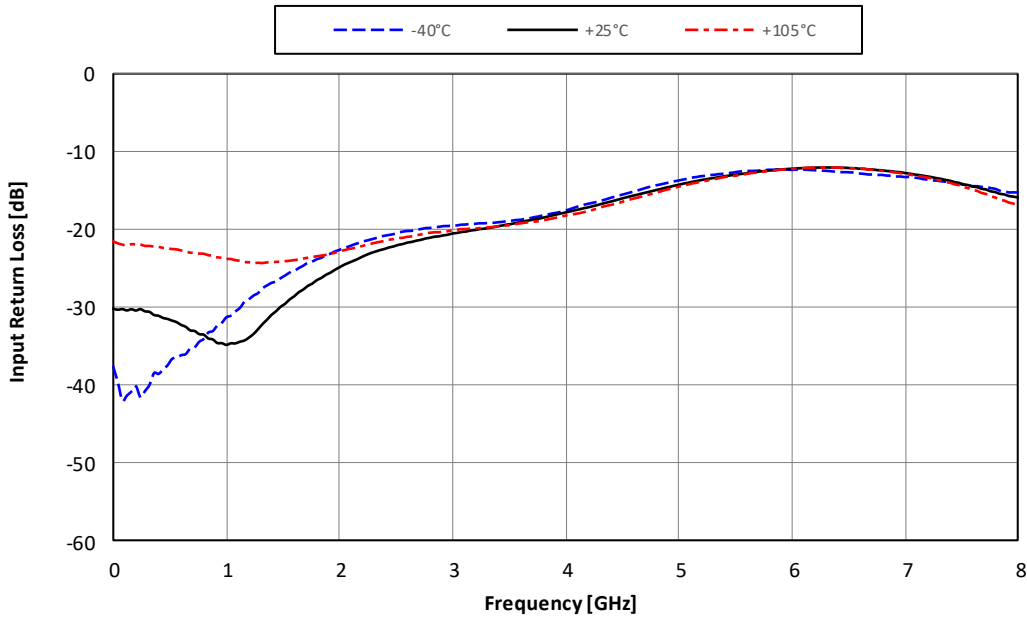
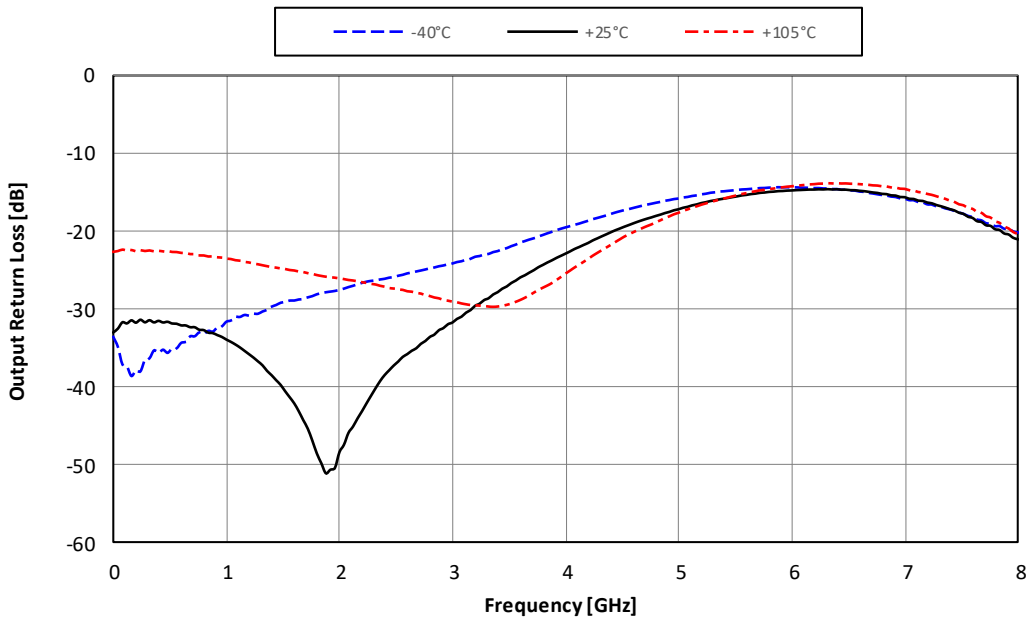


Figure 13. Output Return Loss for 16dB Attenuation Setting vs Temperature



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 14. Relative Phase Error vs Attenuation Setting

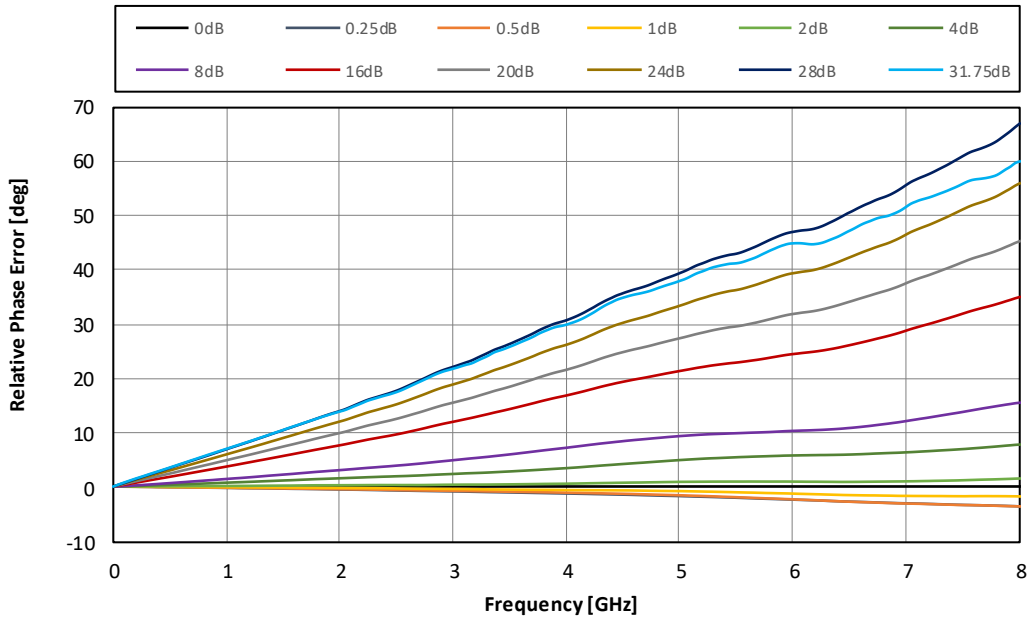
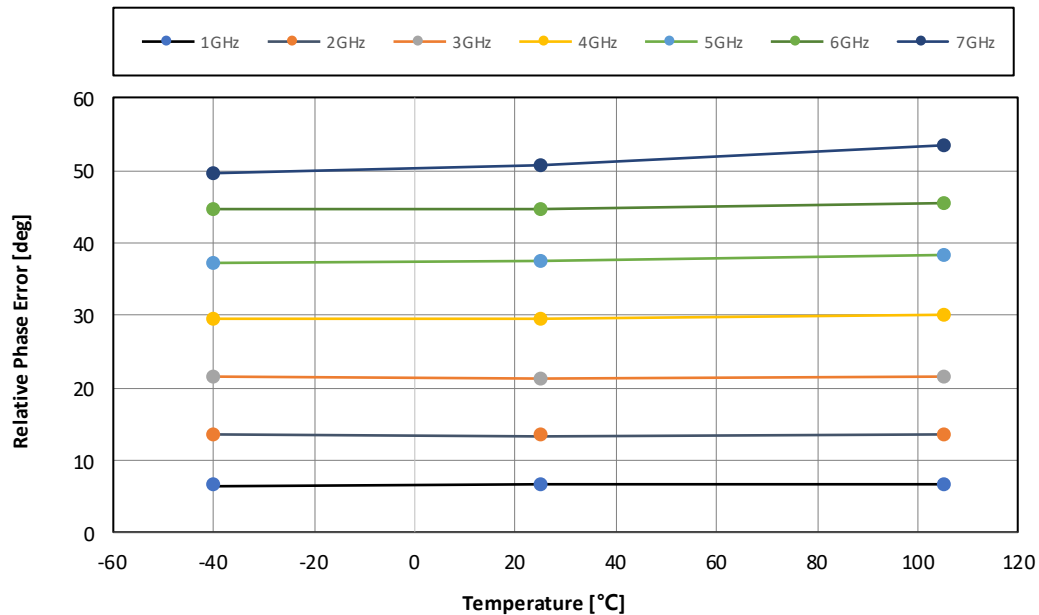


Figure 15. Relative Phase Error for 31.75dB Attenuation Setting vs Frequency



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 16. Attenuation Error @900MHz vs Temperature

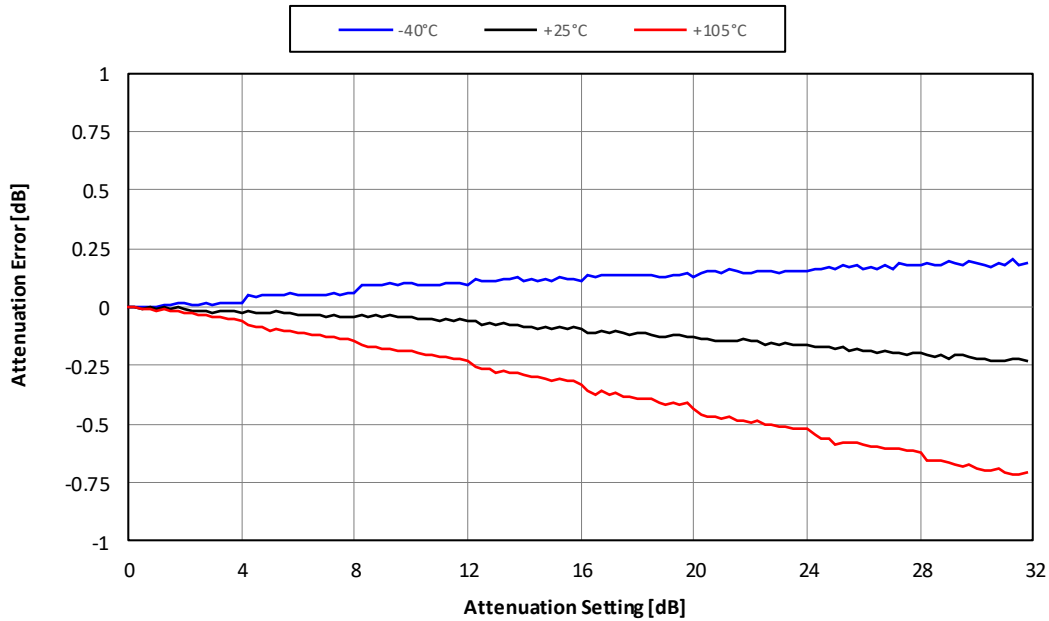
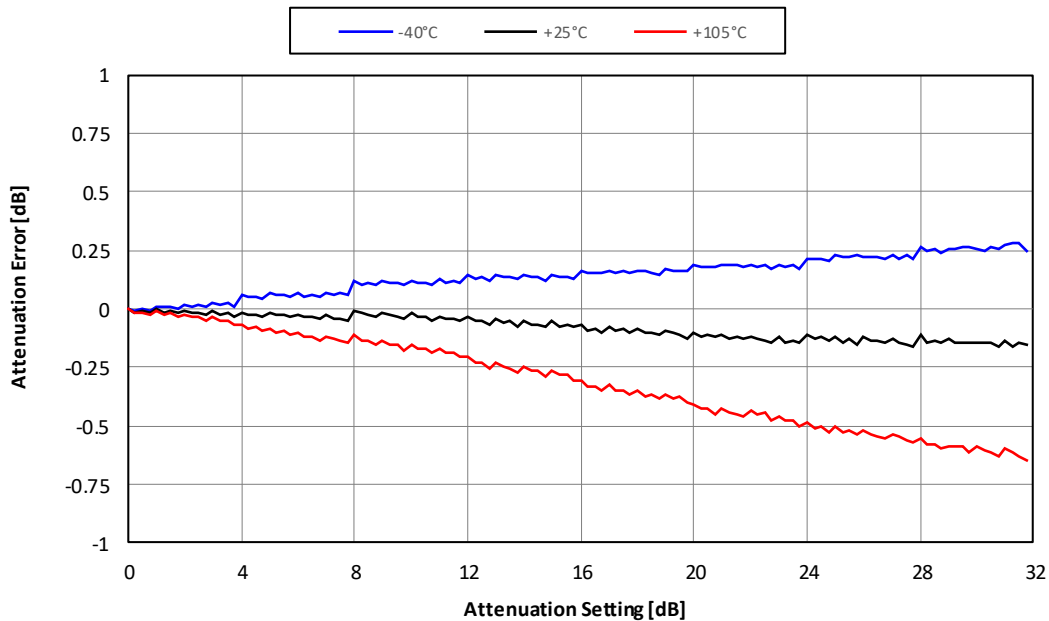


Figure 17. Attenuation Error @1800MHz vs Temperature



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 18. Attenuation Error @2200MHz vs Temperature

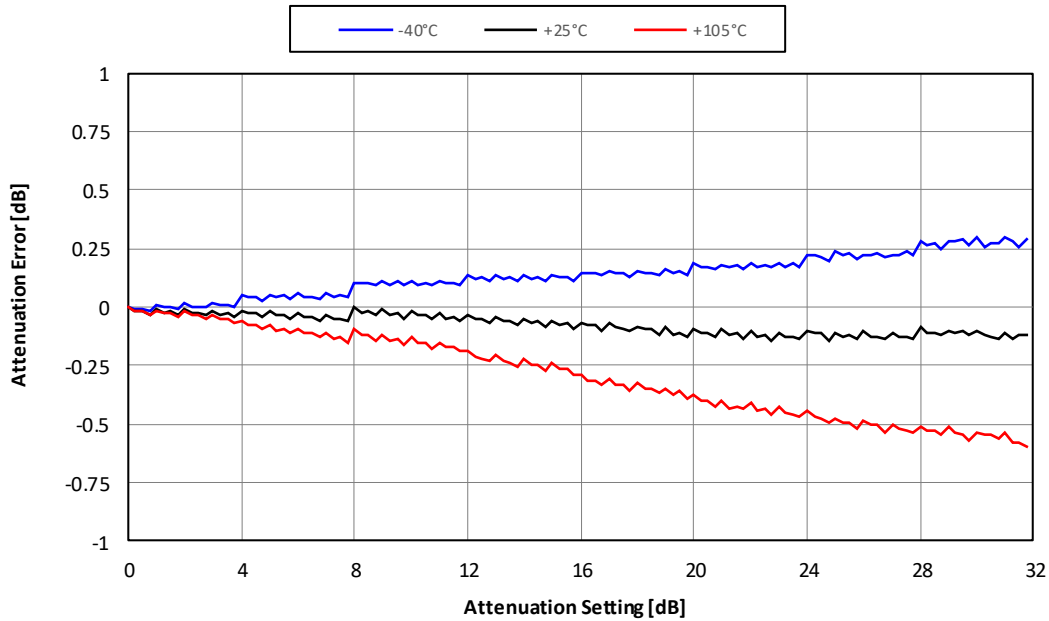
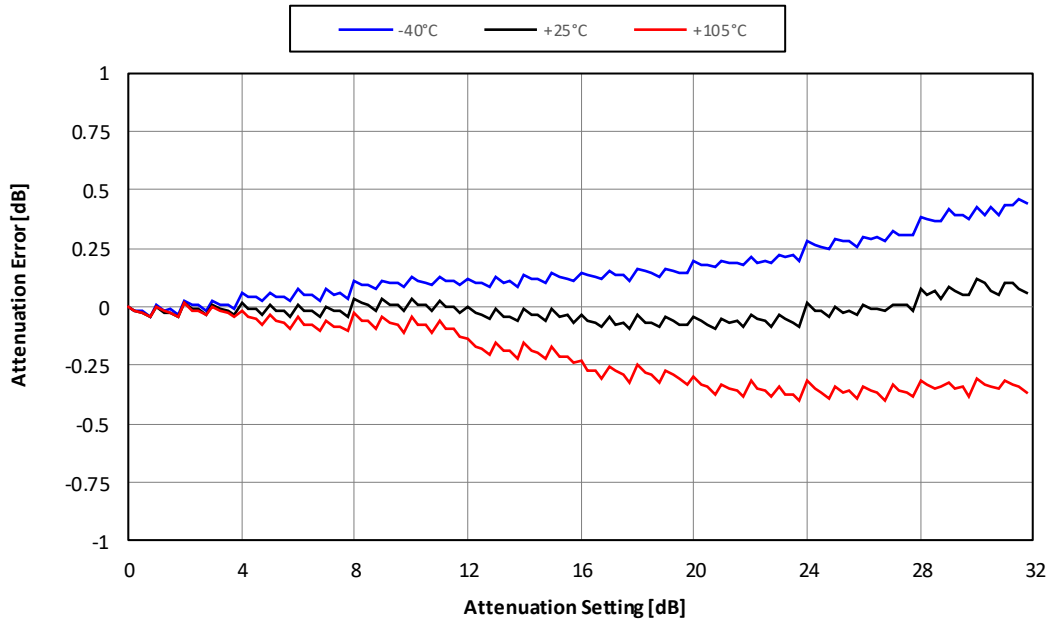


Figure 19. Attenuation Error @3500MHz vs Temperature



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 20. Attenuation Error @4600MHz vs Temperature

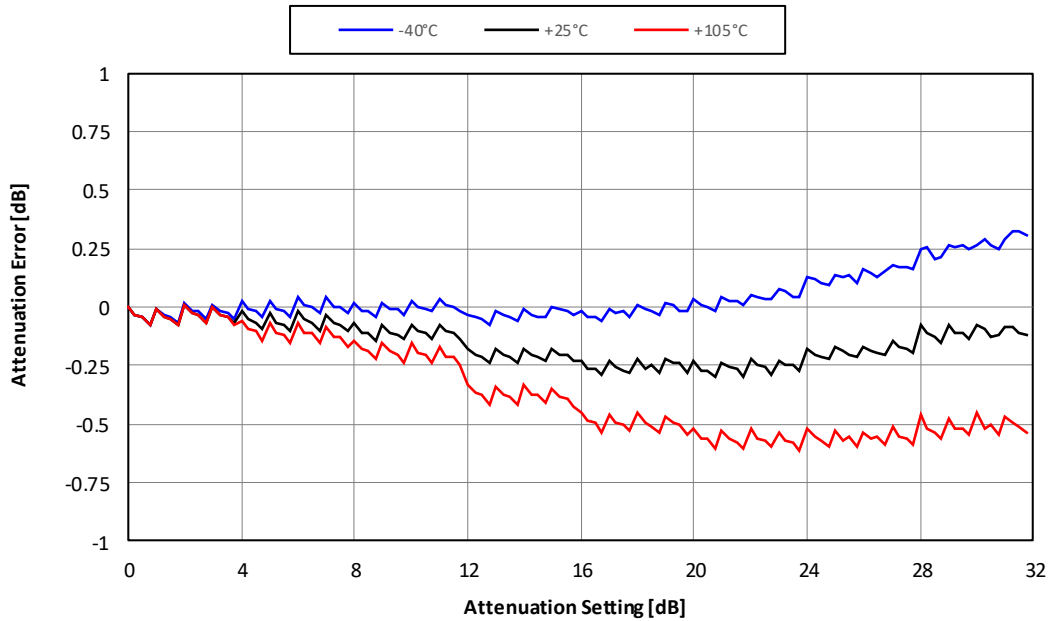
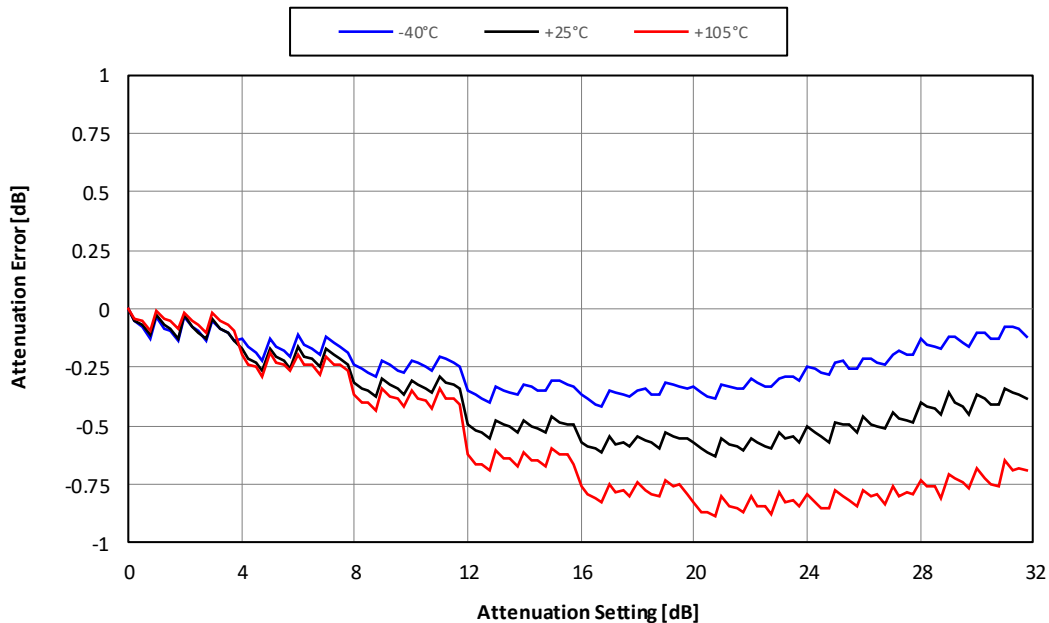


Figure 21. Attenuation Error @5800MHz vs Temperature



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 22. IIP3 @ 2500MHz vs Temperature

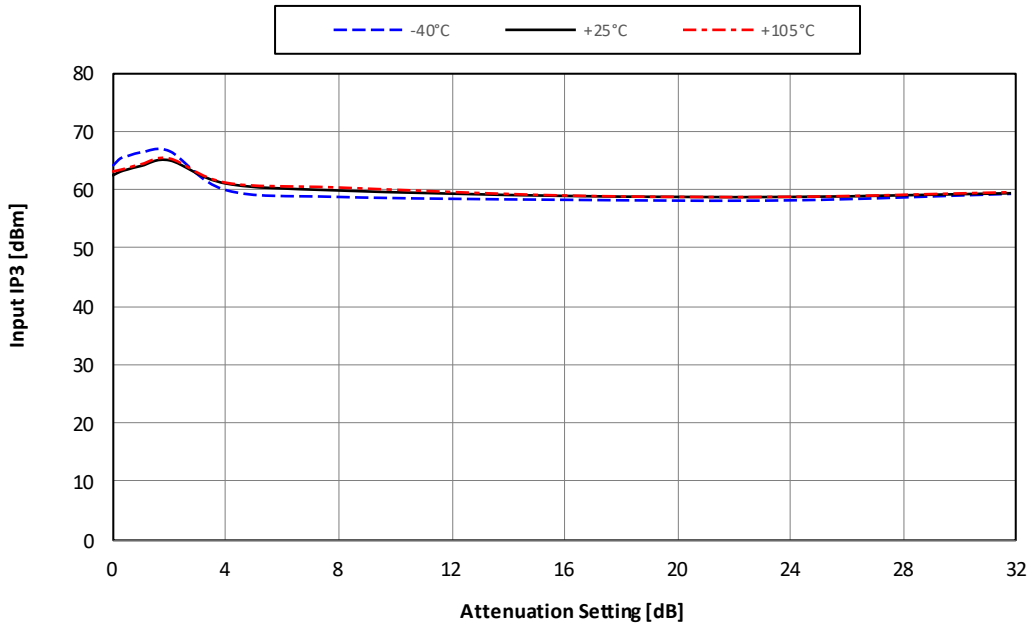
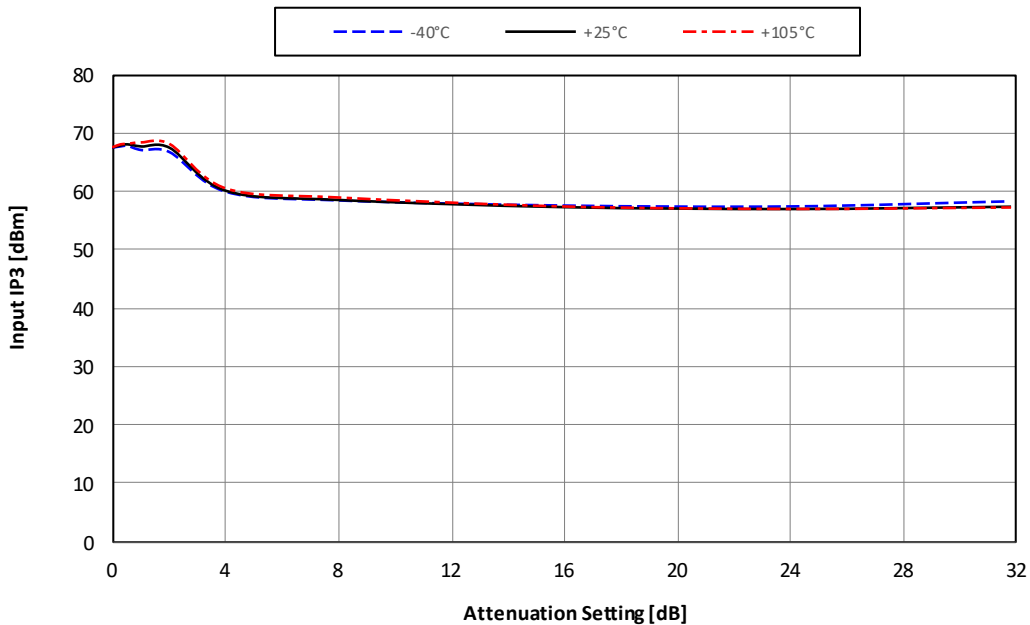


Figure 23. IIP3 @ 3500MHz vs Temperature



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 24. IIP3 @ 4500MHz vs Temperature

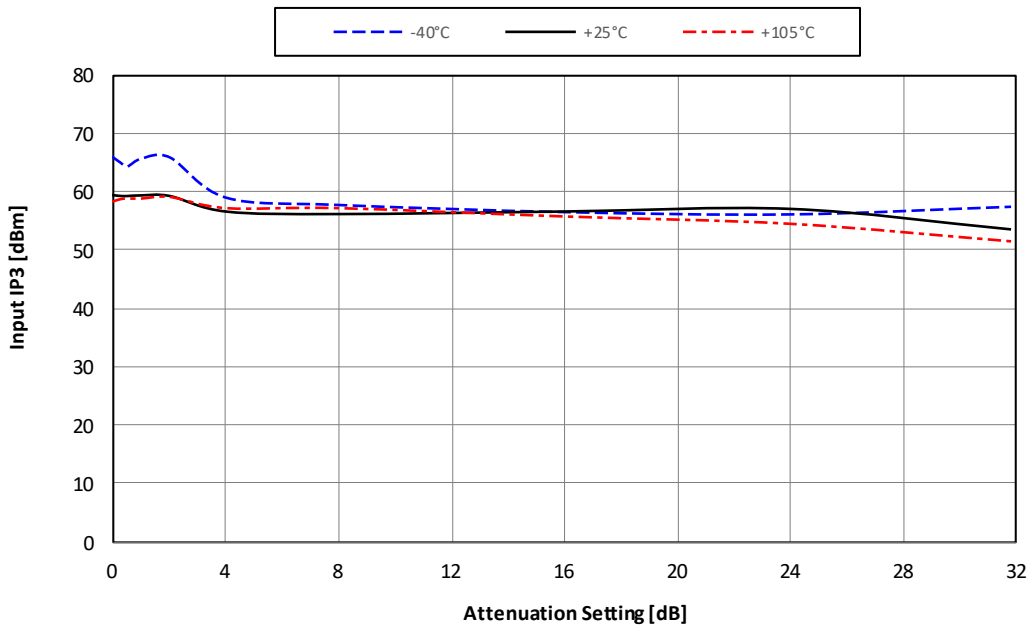
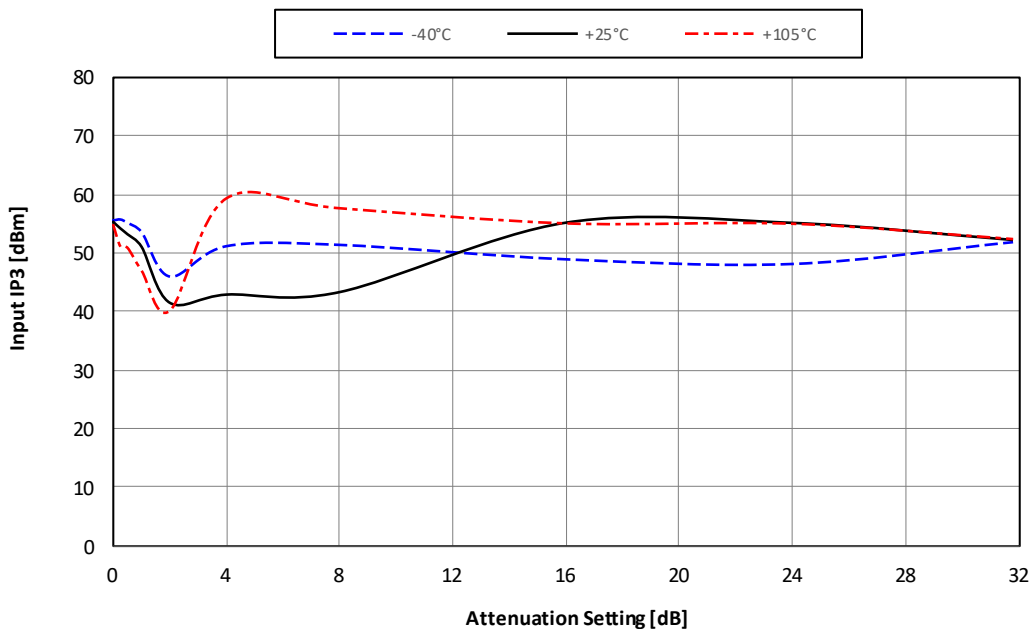


Figure 25. IIP3 @ 6400MHz vs Temperature



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 26. IIP3 @ 7250MHz vs Temperature

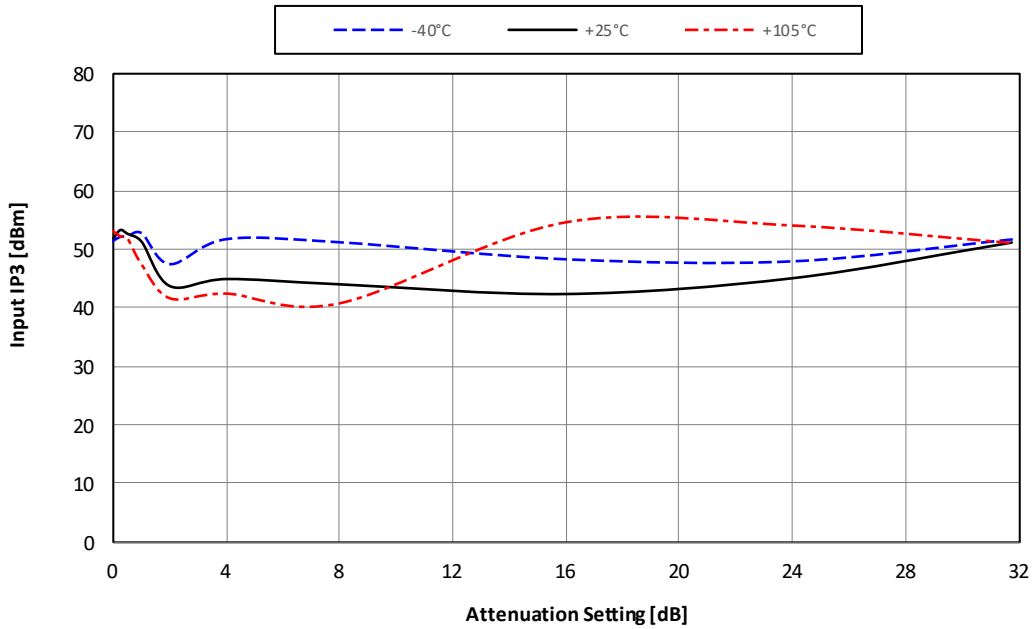
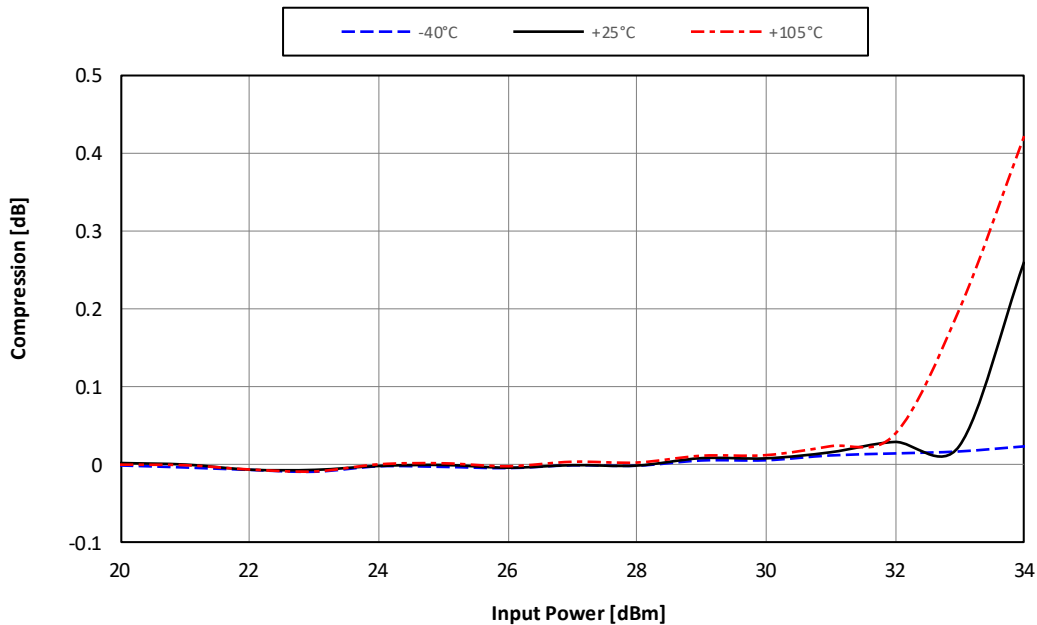


Figure 27. Input 0.1dB Compression @2500MHz vs Temperature



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 28. Input 0.1dB Compression @3500MHz vs Temperature

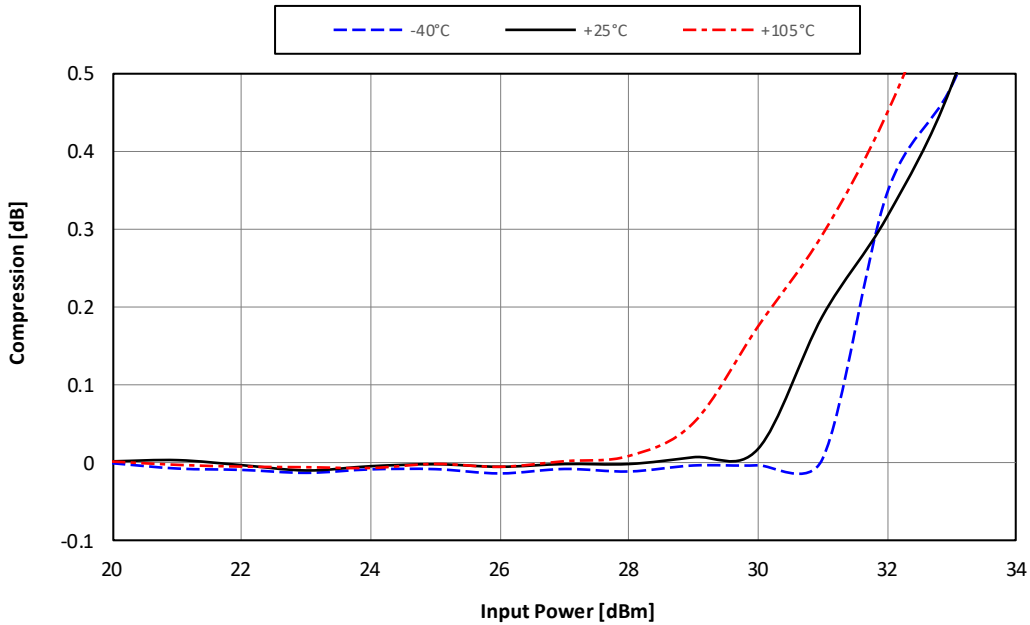
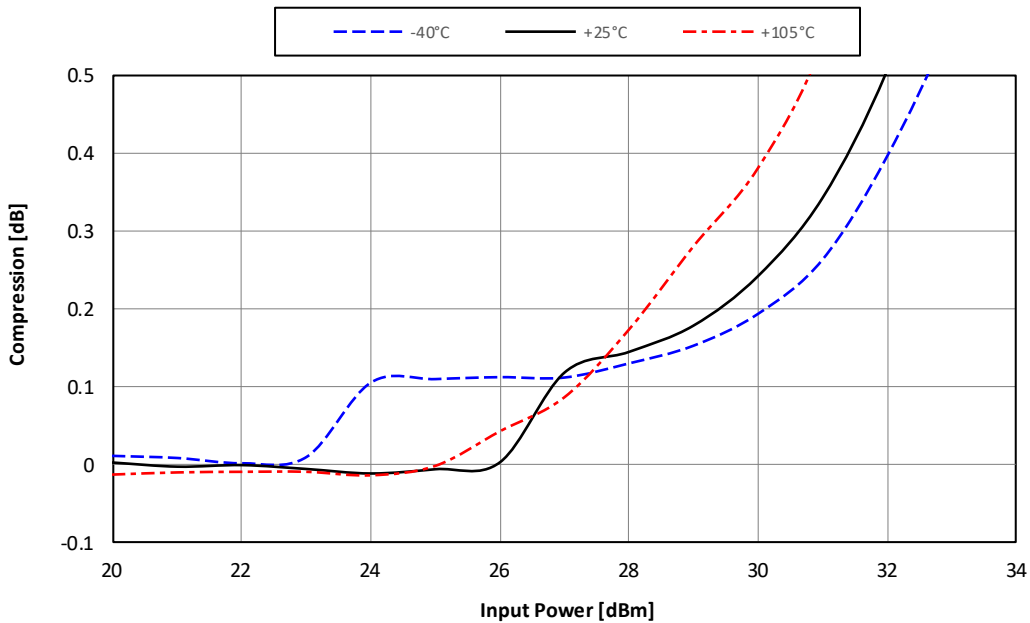


Figure 29. Input 0.1dB Compression @4500MHz vs Temperature



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 30. Input 0.1dB Compression @5500MHz vs Temperature

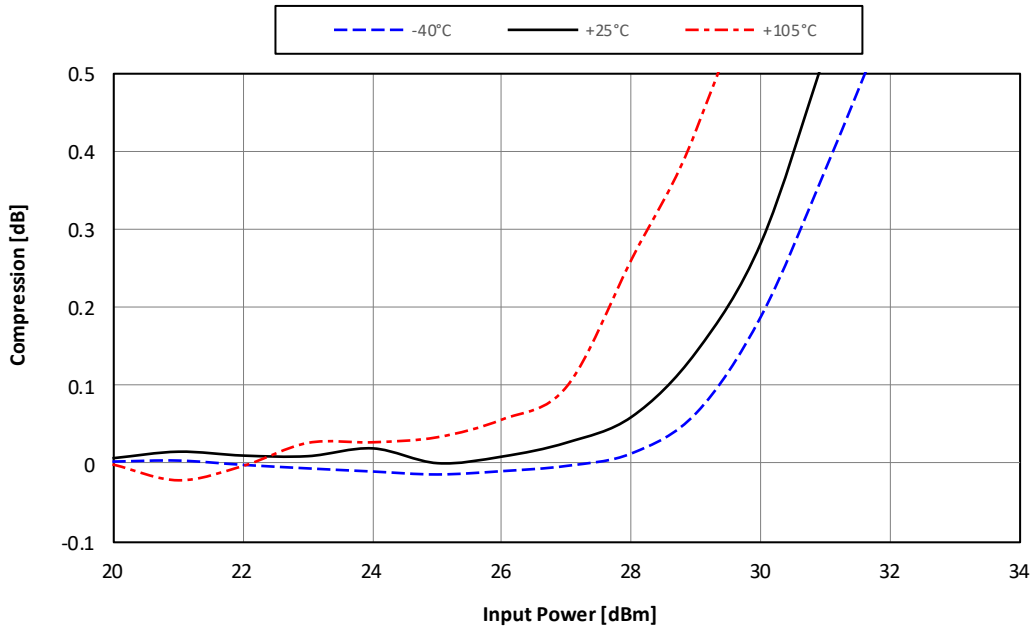
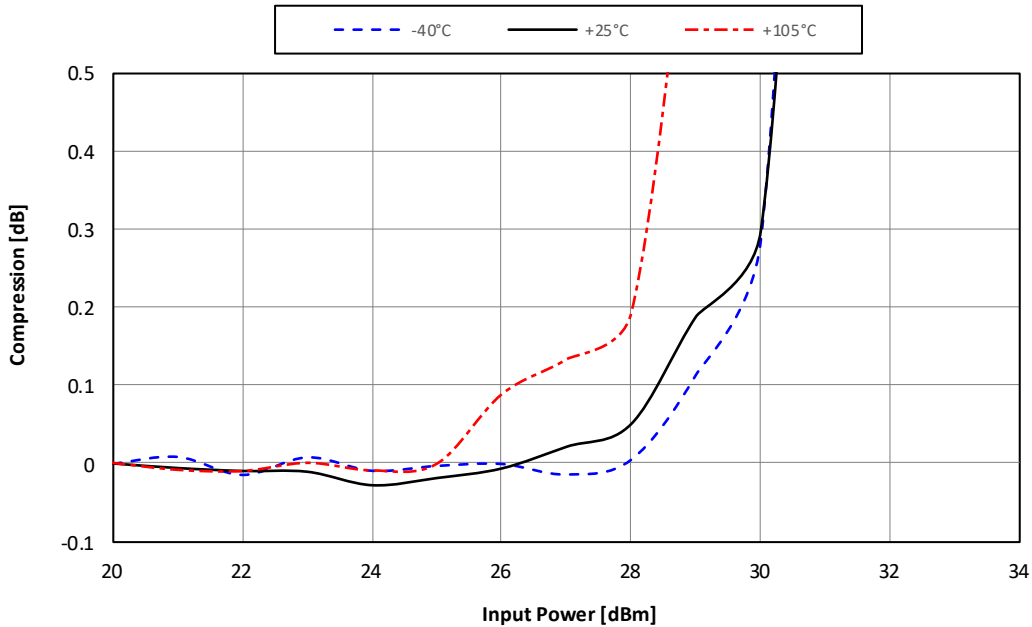


Figure 31. Input 0.1dB Compression @ 7250MHz vs Temperature



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 32. 0.25dB Step Attenuation vs Frequency

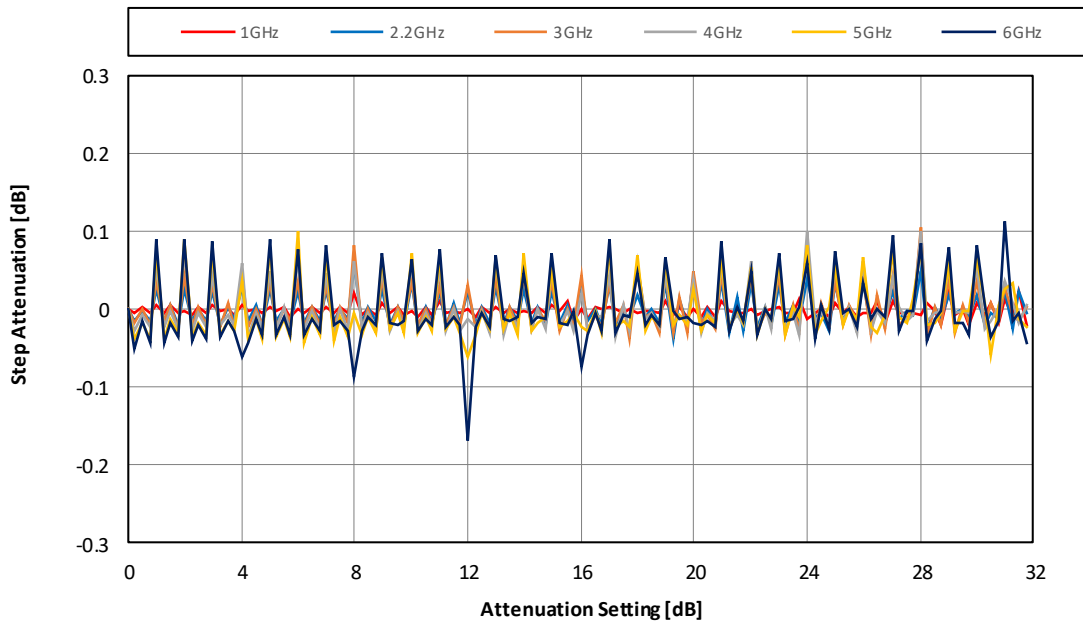
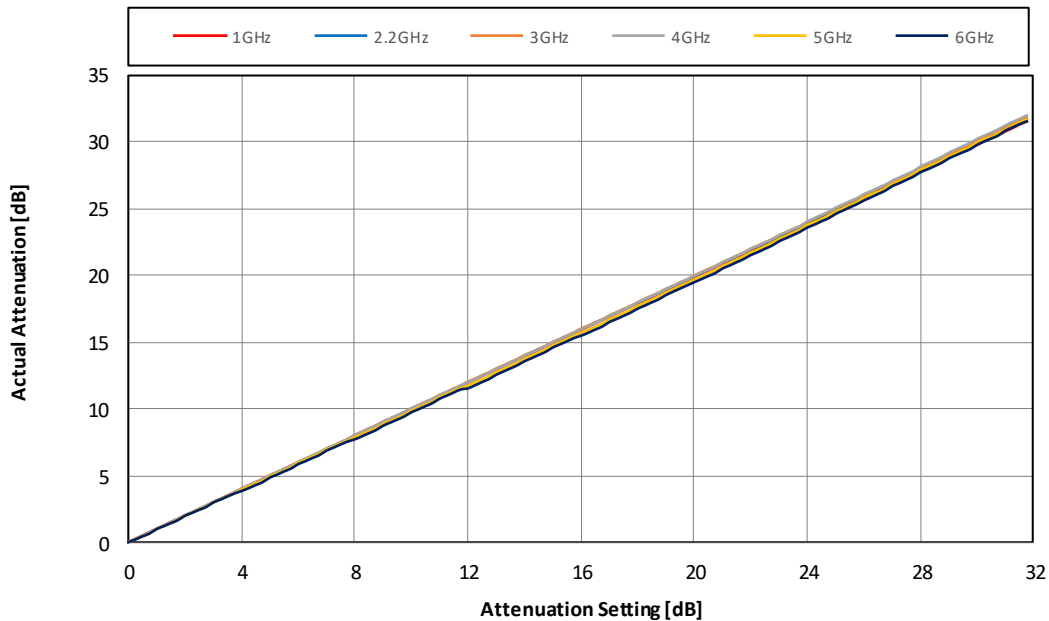


Figure 33. 0.25dB Step Actual Attenuation vs Frequency



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 34. Major State Bit Error vs Attenuation Setting

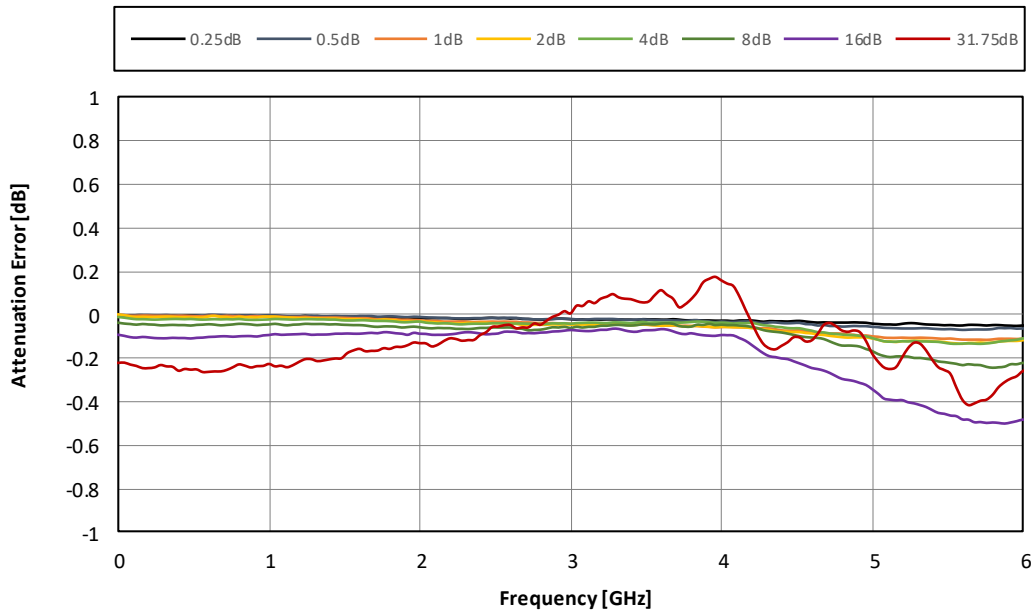
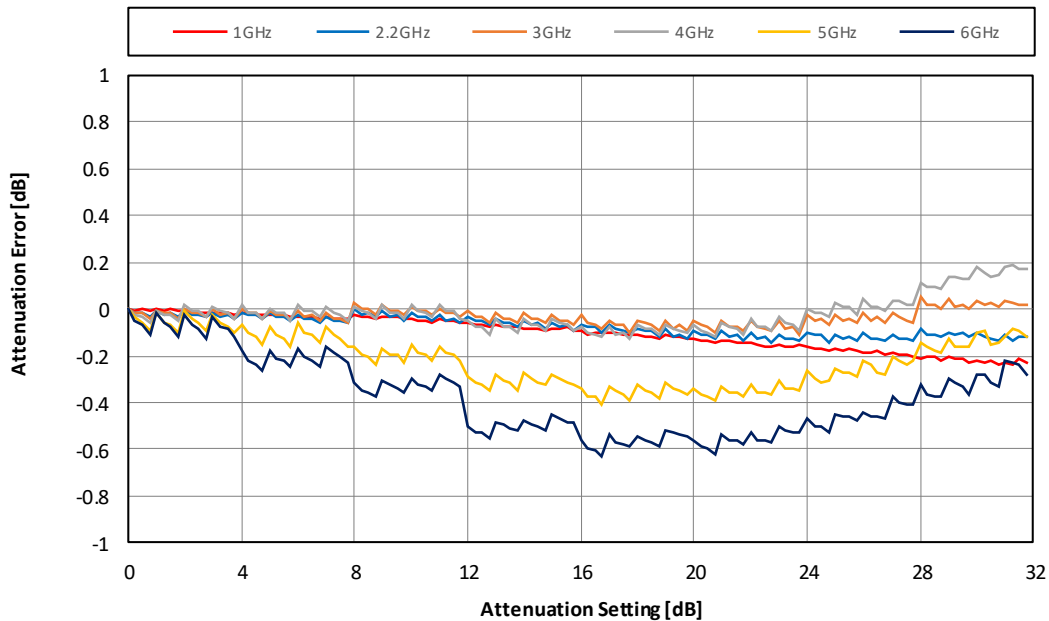


Figure 35. 0.25dB Step Attenuation Error vs Frequency



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 36. 1dB Step Attenuation vs Frequency

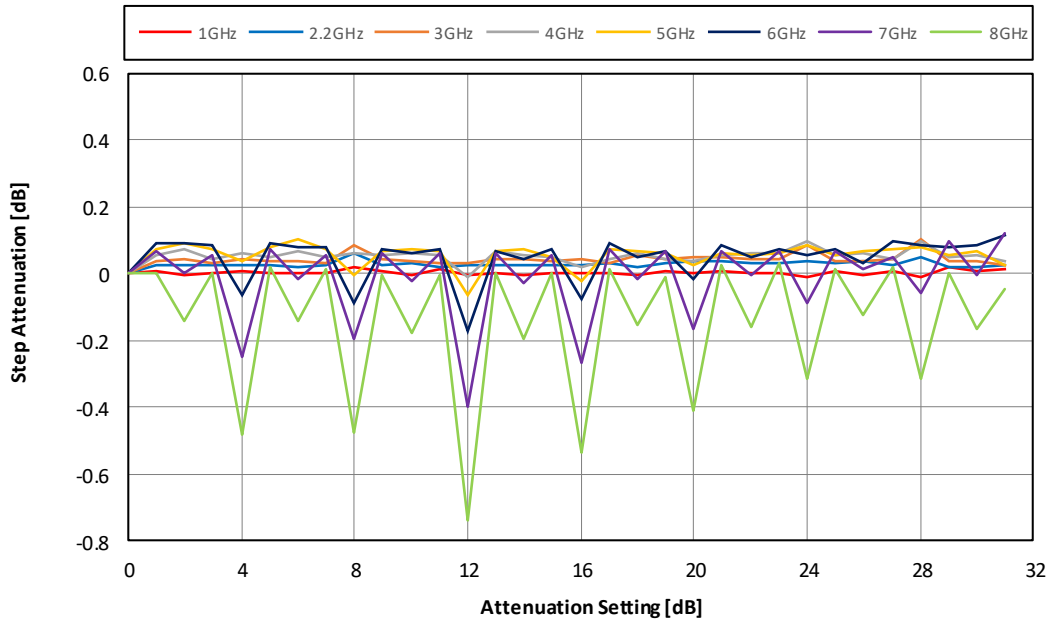
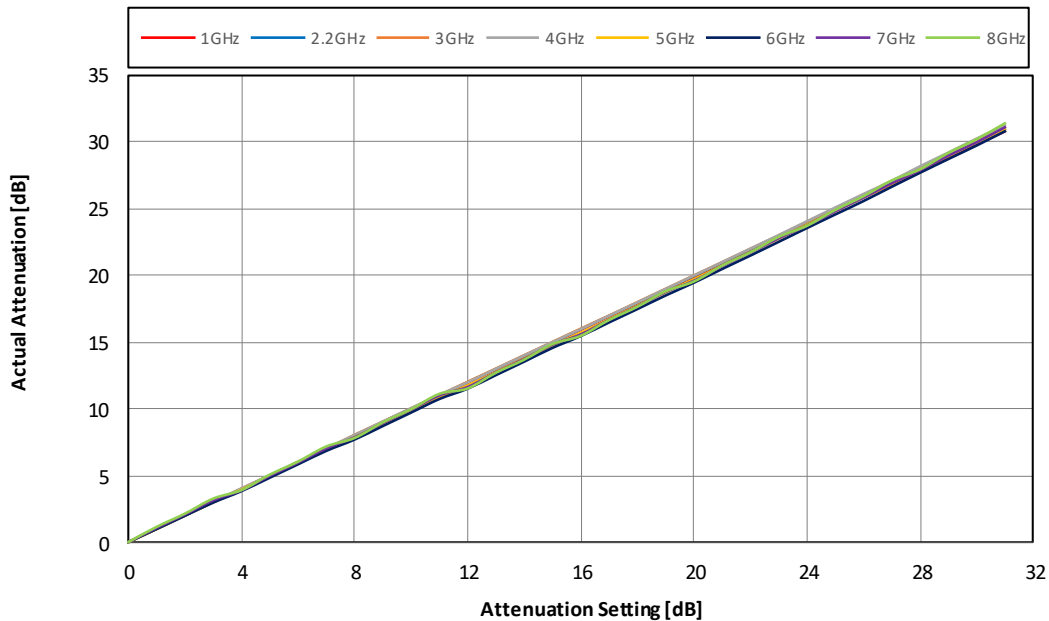


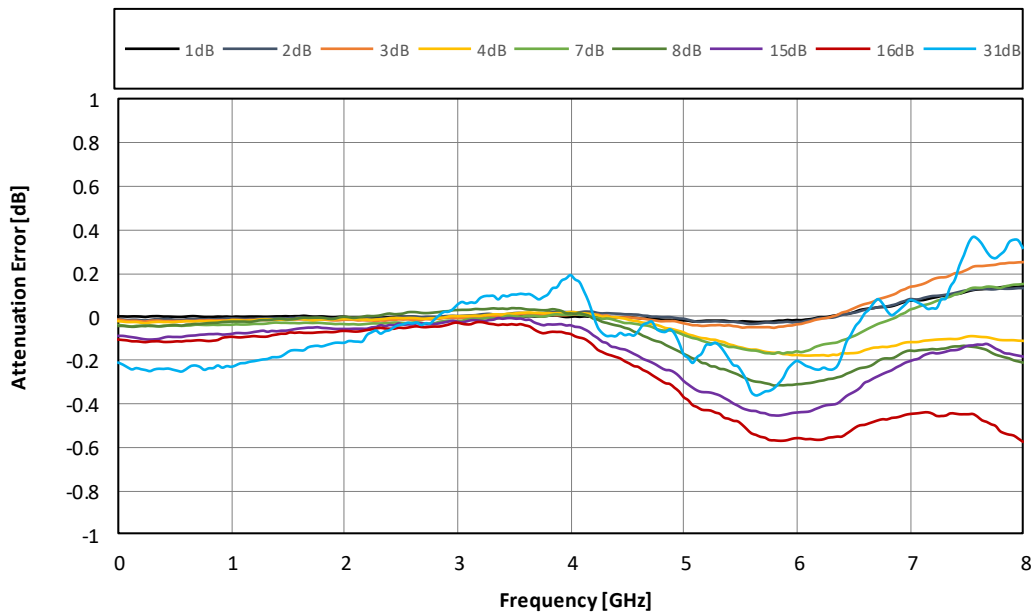
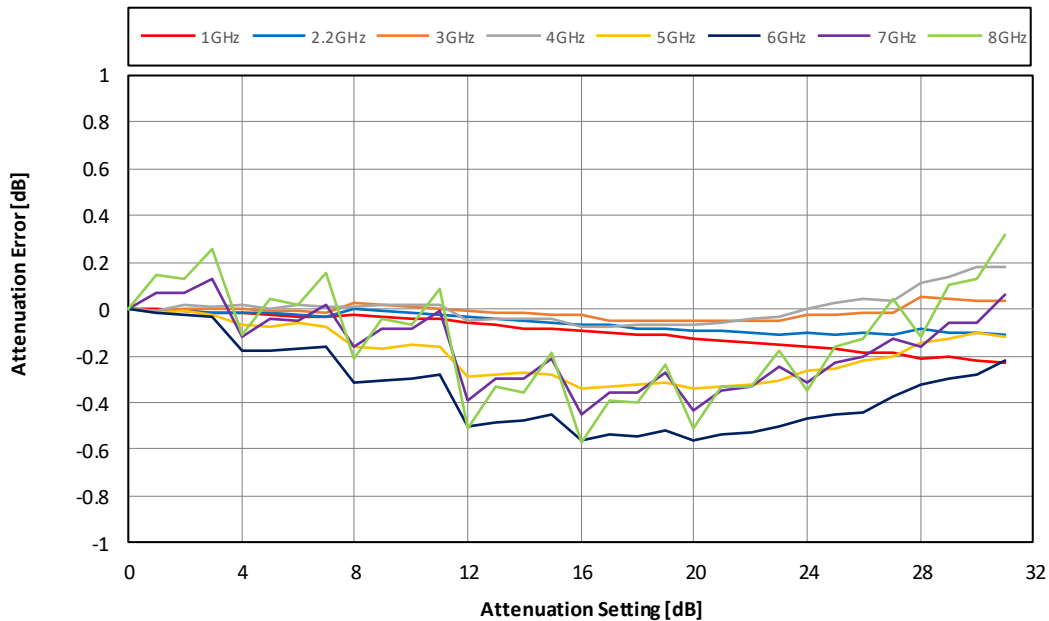
Figure 37. 1dB Step Actual Attenuation vs Frequency



Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

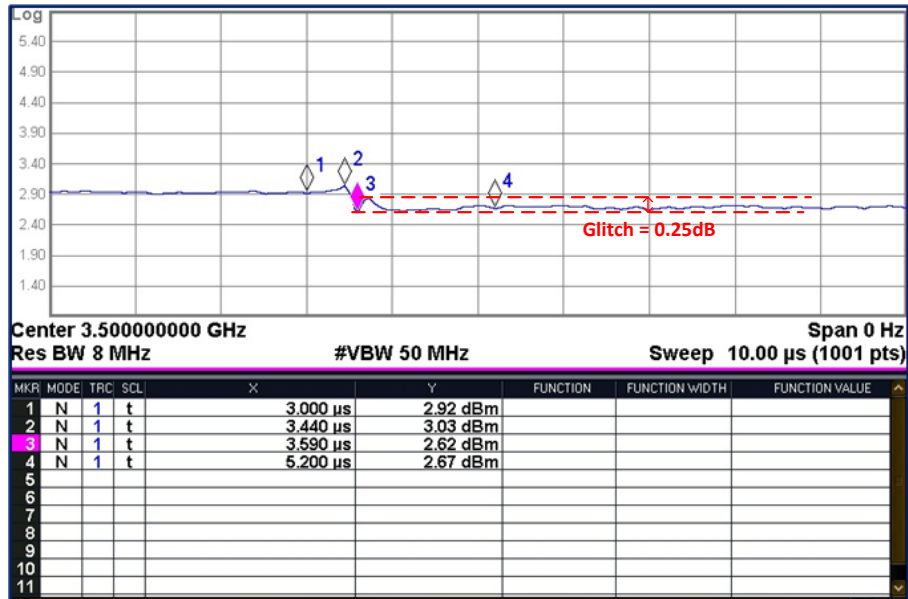
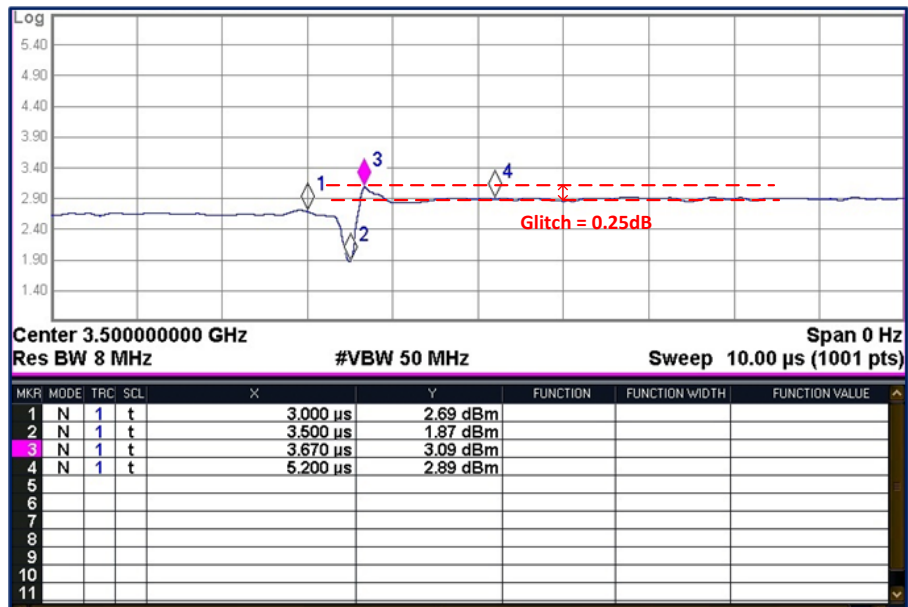
 Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 38. 1dB Major State Bit Error vs Attenuation Setting

Figure 39. 1dB Major Attenuation Error vs Frequency


Preliminary Datasheet

Typical RF Performance Plot - BDA4710 EVK - PCB

 Typical Performance Data @ 25°C and $V_{DD} = 3.3V$, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 40. Attenuation Transient(15.75-16dB, Pin=18dBm)

Figure 41. Attenuation Transient(16-15.75dB, Pin=18dBm)


Preliminary Datasheet

BDA4710 Evaluation board Kit Description

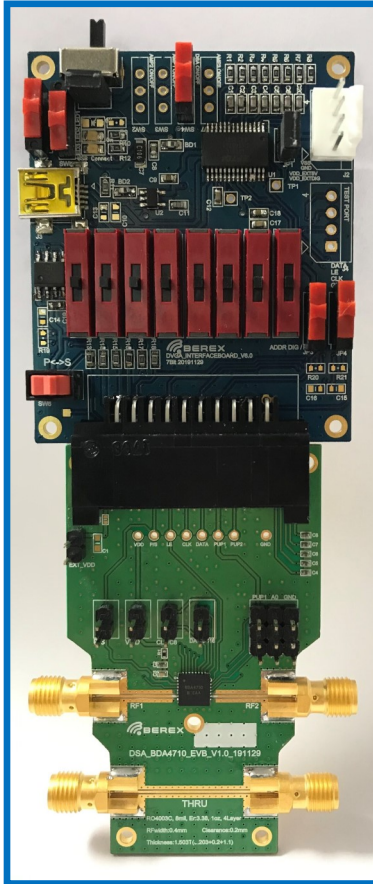


Figure 42. BDA4710 EVK

Evaluation board Kit Introduction

BDA4710 Evaluation Kit is made up of a combination of an RF board and an interface board

The schematic of the BDA4710 evaluation RF board is shown in Figure 34. The BDA4710 evaluation RF board is constructed of a 4-layer material with a copper thickness of 0.7 mil on each layer. Every copper layer is separated with a dielectric material. The top dielectric material is 8 mils RO4003. The middle and bottom dielectric materials are FR-4, used for mechanical strength and overall board thickness of approximately 1.63mm.

BDA4710 Evaluation INTERFACE board is assembled with a SP3T switches(D0~D6,LE), SP2T mechanical switch (P/S), and several header & switch.

Evaluation Board Programming Using USB Interface

In order to evaluate the BDA4710 performance, the Application Software has to be installed on your computer. And The DSA application software GUI supports Latched Parallel and Serial modes. software can be downloaded from BeRex's website

Serial Control Mode

- Set the Address Jumper (A0, A1, A2) to HIGH or LOW (Refer to Address Table 7)
- Connect directly the Evaluation INTEFRACE board USB port(J3) to PC
- Set the direction of P<->S Switch to S direction (P/S Logic HIGH)
- Set the D0~D6, LE switch to the middle position.
- Operate the 0~31.75dB attenuation state in GUI and then control the DSA

Latched Parallel Control Mode

- Connect directly the Evaluation INTEFRACE board USB port(J3) to PC
- Set the direction of P<->S Switch to P direction (P/S Logic LOW)
- Set the D0~D6, LE switch to the middle position.
- Operate the 0~31.75dB attenuation state in GUI and then control the DSA

Direct Parallel Control Mode

- Set the direction of P<->S Switch to P direction (P/S Logic LOW)
- Set LE switch to the LOW Position
- For the setting to attenuation state, D0~D6 switches can be combined in manually program, refer to Table 9.

Please refer to user manual for more detailed operation method of BDA4710 EVK.

BDA4710 Evaluation board Kit Description

Figure 43. Evaluation Board Kit Schematic Diagram

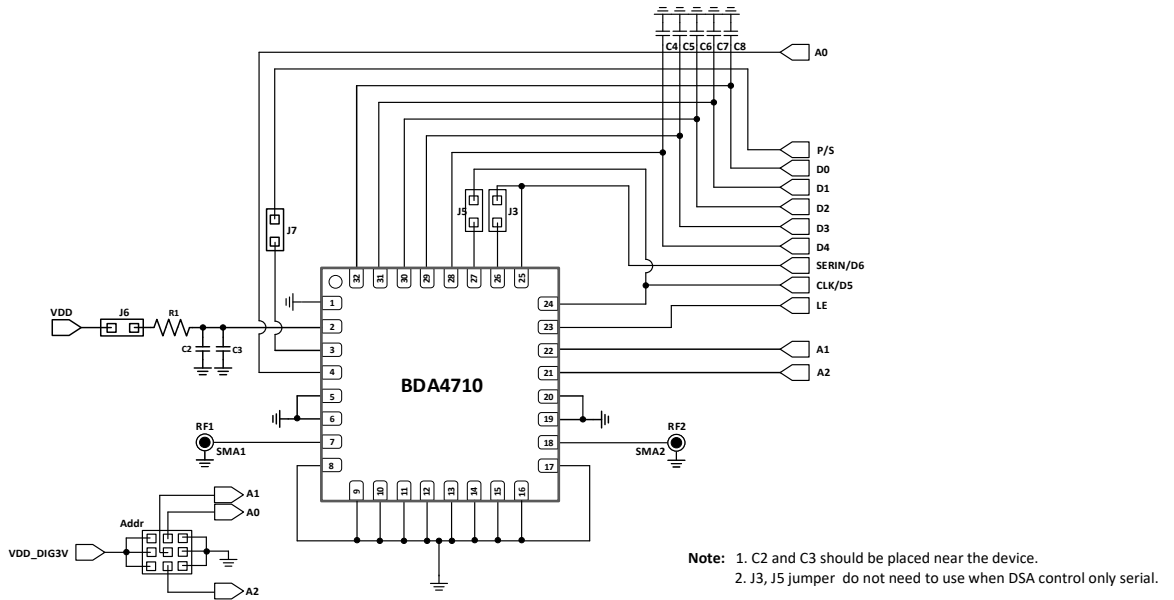


Figure 44. Evaluation Board PCB Layout Information 50Ω

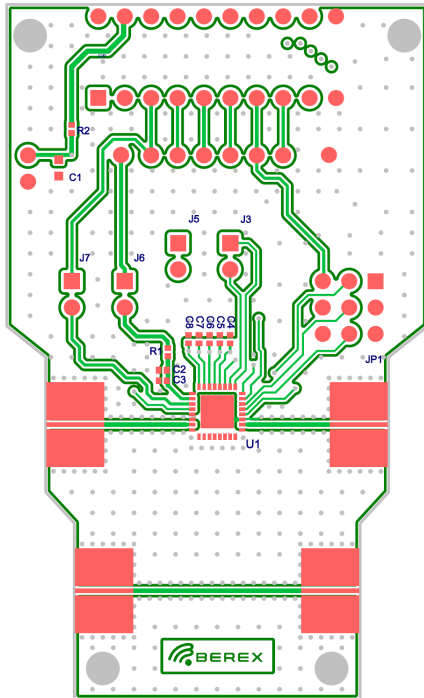
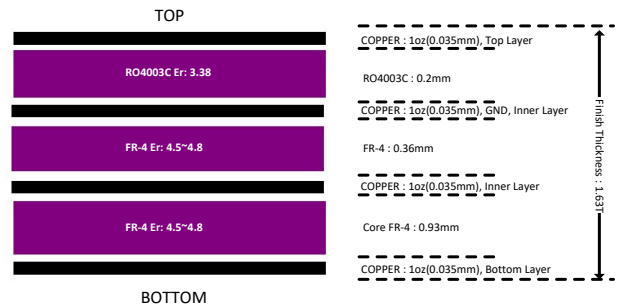


Table 11. Bill of Material - Evaluation Board

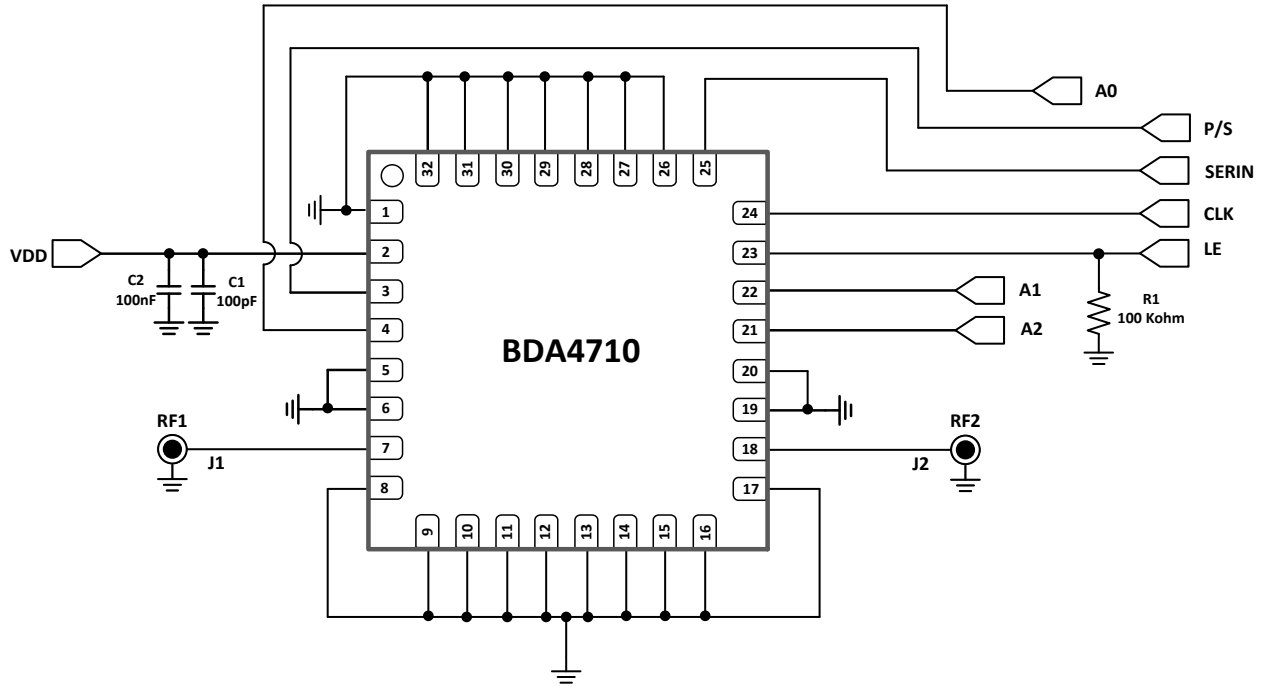
| No. | Ref Des | Part Qty | Value | Description | Remark |
|-----|------------|----------|-------|---------------------------------|--------|
| 1 | C3,C4-C8 | 6 | 100pF | CAP, 0402, CHIP Ceramic, ±0.25% | |
| 2 | C2 | 1 | 100nF | CAP, 0402, CHIP Ceramic, ±0.25% | |
| 3 | R1 | 1 | 0 ohm | RES, 0402, CHIP, ±5% | |
| 4 | C1,R2 | 2 | NC | | |
| 5 | SMA1, SMA2 | 2 | CON | SMA END LAUNCH | |
| 6 | U1 | 1 | Chip | DSA, BDA4710 QFN5x5 32L | |

Figure 45. Evaluation Board PCB Layer Information 50Ω



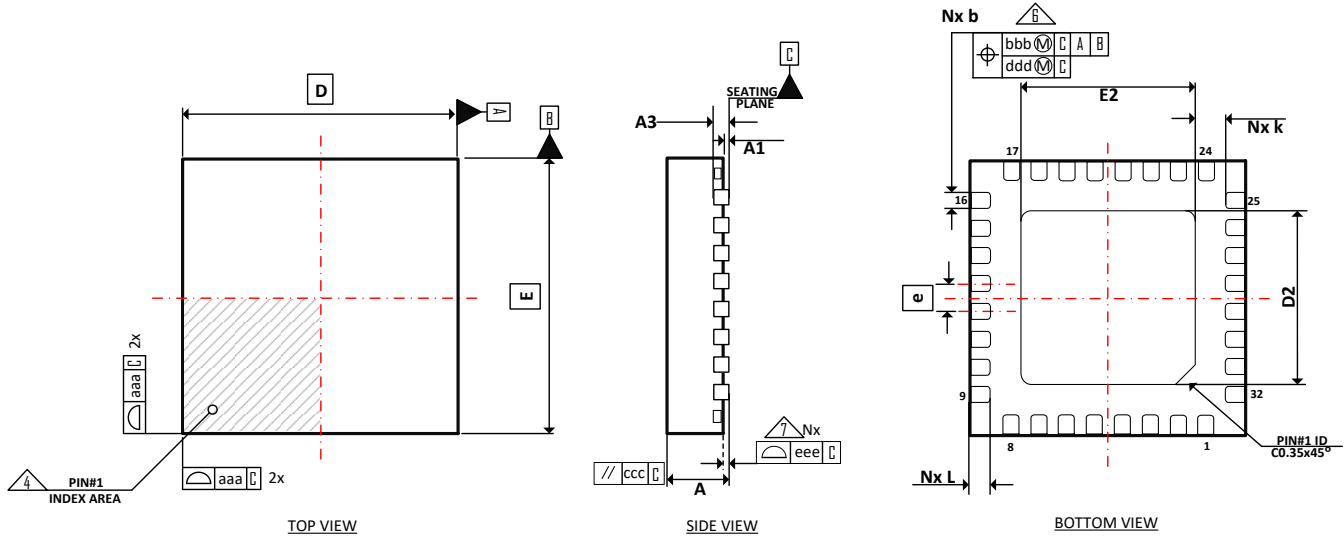
Preliminary Datasheet

Figure 46. Recommended Serial mode Application Schematic



- Note:**
1. C1 and C2 should be placed near the device.
 2. Recommended to add pull-down at the LE pin.
 3. Addressable Pin A0,A1,A2 can be set according to the specified address. If the specified address is 000, All addressable pin(A0,A1,A2) should be grounded.

Figure 47. Packing Outline Dimension



| Dimension Table | | | | |
|-----------------|-----------|-----------|---------|------|
| Symbol | Thickness | | | NOTE |
| | MINIMUM | NOMINAL | MAXIMUM | |
| A | 0.8 | 0.9 | 1 | |
| A1 | 0 | 0.02 | 0.05 | |
| A3 | --- | 0.203 Ref | --- | |
| b | 0.2 | 0.25 | 0.3 | 6 |
| D | | 5.0 BSC | | |
| D2 | 3.05 | 3.10 | 3.15 | |
| E | | 5.0 BSC | | |
| E2 | 3.05 | 3.10 | 3.15 | |
| e | | 0.5 BSC | | |
| K | 0.2 | --- | --- | |
| L | 0.3 | 0.4 | 0.5 | |
| aaa | | 0.05 | | |
| bbb | | 0.1 | | |
| ccc | | 0.1 | | |
| ddd | | 0.05 | | |
| eee | | 0.08 | | |
| N | | 32 | | 3 |
| ND | | 8 | | 5 |
| NE | | 8 | | 5 |
| NOTES | | 1, 2 | | |

NOTE :

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.

2. All dimensions are in millimeters.

3. N is the total number of terminals.

4. The location of the marked terminal #1 identifier is within the hatched area.

5. ND and NE refer to the number of terminals on each D and E side respectively.

6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.

7. Coplanarity applies to the terminals and all other bottom surface metallization

Figure 48. Recommend Land Pattern

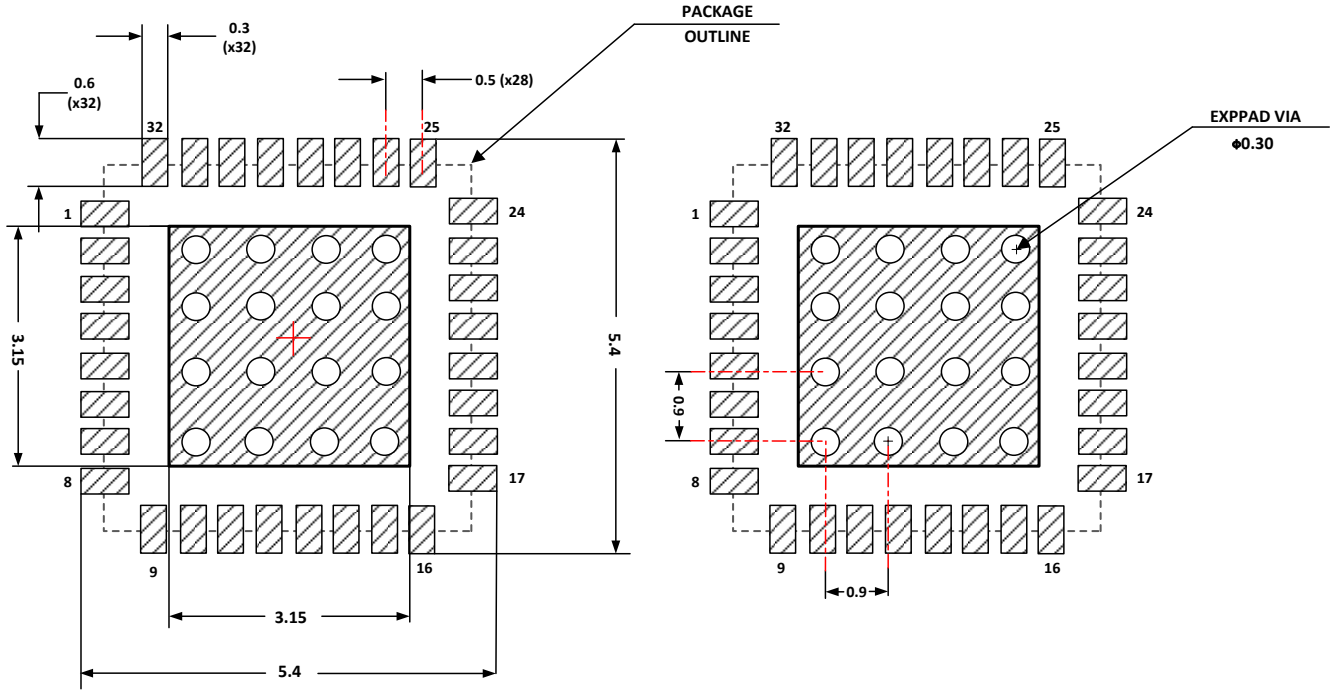


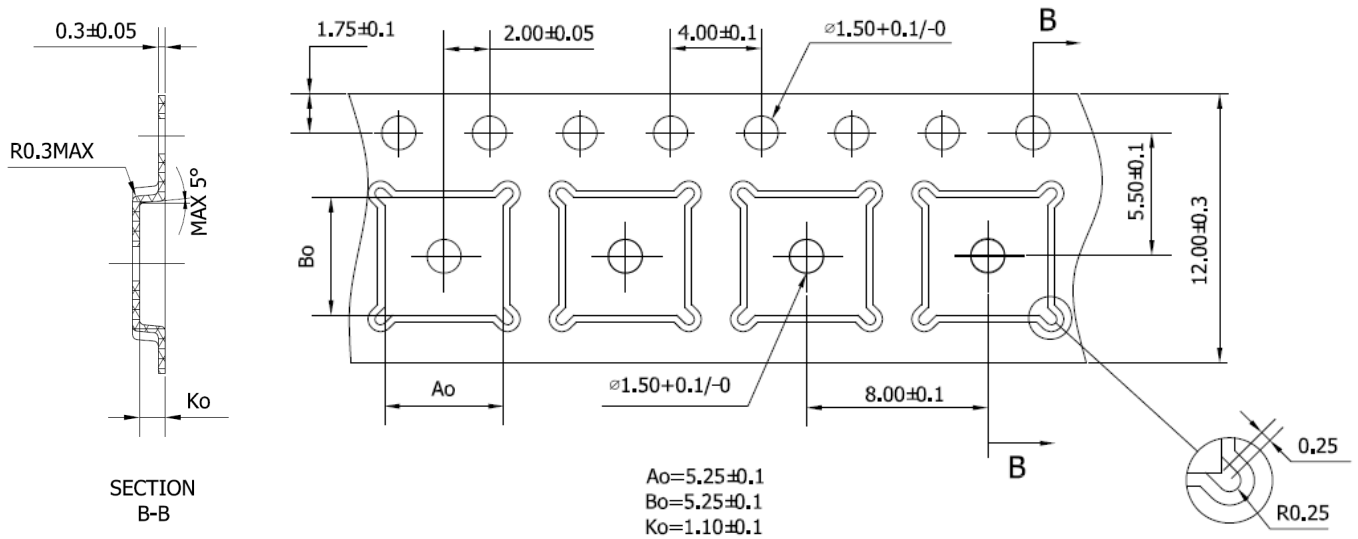
Figure 49. Package Marking



| Marking information: | |
|----------------------|-------------|
| BDA4710 | Device Name |
| YY | Year |
| WW | Work Week |
| XX | LOT Number |

Preliminary Datasheet

Figure 50. Tape & Reel



NOTES:

- 1 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
- 2 CAMBER IN COMPLIANCE WITH EIA 481
- 3 POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Packaging information:

| | |
|---------------------|-------|
| Tape Width | 12mm |
| Reel Size | 7inch |
| Device Cavity Pitch | 8mm |
| Devices Per Reel | 1k |

Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating: Class 1C
Value: 1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JS-001-2017

ESD Rating: Class C4
Value: 1000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating: Level 1 at +260°C convection reflow
Standard: JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO CAGE code:

| | | | | |
|---|---|---|---|---|
| 2 | N | 9 | 6 | F |
|---|---|---|---|---|